Comparative Review of SiC and GaN Power Devices for High-Frequency DC–DC Converters

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Abstract

This structured comparative review examines silicon carbide (SiC) and gallium nitride (GaN) wide-bandgap semiconductor (WBG) devices in high-frequency direct current (DC)-DC converters. Twenty-two peer-reviewed publications and industry reports, eleven from 2021–2026, were evaluated against criteria covering material physics, switching dynamics, converter topology performance, electromagnetic compatibility, thermal management, and reliability. A silicon-referenced normalized matrix combines material-, device-, converter-, and market-level indicators with topology mapping, electromagnetic interference (EMI) spectral comparison, and reliability physics. Reported DC-DC converter data show that GaN high electron mobility transistor (HEMT) designs reach the highest surveyed efficiency (98.5% in a 10 kW phase-shifted full-bridge above 150 kHz) and superior power density below 650 V, whereas SiC metal-oxide-semiconductor field-effect transistor (MOSFET) devices remain preferred above 1200 V and under high thermal stress; these values are topology-specific. Parasitic inductance, conducted EMI reaching 400 MHz, and packaging remain the principal barriers to SiC MOSFET and GaN HEMT adoption in power electronics.

Keywords: wide-bandgap semiconductor, SiC MOSFET, GaN HEMT, DC-DC converter, power electronics

1. Introduction

The global imperative toward energy efficiency and power miniaturization has catalyzed a fundamental technological transition in power electronics. Legacy silicon (Si) semiconductors—specifically insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs)—have defined power conversion systems since their commercial introduction in the mid-twentieth century. However, silicon's intrinsically narrow bandgap of 1.1 eV imposes hard physical limits on its operational temperature ceiling, blocking voltage capability, and maximum switching frequency [1].

These limitations are becoming increasingly consequential as the demands of modern electrified systems intensify. Electric vehicles (EVs), operating on 800 V battery architectures, require traction inverters and onboard chargers (OBCs) capable of handling kilovolt-class blocking voltages at elevated temperatures. Data center power delivery networks seek conversion efficiencies exceeding 99% with unprecedented power densities [2]. Fifth-generation (5G) telecommunications base stations mandate radio-frequency power amplifiers capable of gigahertz-range operation. In each of these sectors, silicon's physical constraints represent a fundamental bottleneck [2].

Wide-bandgap (WBG) semiconductor materials, principally silicon carbide (SiC) and gallium nitride (GaN), have emerged as transformative solutions. Both materials share bandgap energies approximately three times that of silicon (3.26 eV for 4H-SiC and 3.4 eV for GaN), critical electric fields (Ec) nearly an order of magnitude higher (3.0 MV/cm and 3.3 MV/cm,

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respectively), and maximum operating temperatures well exceeding 200℃ [3]. These attributes collectively enable direct current (DC)-DC converters to operate at dramatically higher switching frequencies—transitioning from the conventional tens of kilohertz domain into the megahertz regime—with a corresponding reduction in passive component volume and overall system weight [4].

Despite sharing the broad classification of WBG materials, SiC and GaN exhibit distinctly different physical architectures, electro-thermal profiles, and commercially viable application spaces. SiC power devices are constructed predominantly as vertical MOSFET structures, leveraging bulk crystal volume for heat distribution and high-voltage blocking above 1200 V. Conversely, GaN devices exploit a lateral high electron mobility transistor (HEMT) architecture featuring a two-dimensional electron gas (2DEG) channel at the AlGaN/GaN heterojunction interface. This architecture yields electron mobilities approaching 2000 $cm^2/V \cdot s$, a property that grants GaN unparalleled switching agility in the sub-650 V domain [4].

While the theoretical superiority of WBG materials over silicon is well-established in the solid-state physics literature, practical deployment in high-frequency DC-DC converters introduces complex system-level engineering challenges. The extreme dv/dt and di/dt transients inherent to WBG switching exacerbate electromagnetic interference (EMI), stimulate parasitic inductances within printed circuit board (PCB) layouts, and impose severe thermo-mechanical stresses on semiconductor packaging structures [5].

1.1 Research gap and motivation

Existing comparative literature on SiC and GaN devices largely addresses individual aspects such as material characterization, specific converter prototypes, or isolated reliability studies. Foundational WBG surveys [4, 17] predate the recent generation of commercial 650 V GaN HEMTs and 1200 V SiC MOSFETs and do not provide converter-level benchmarking; dedicated reliability reviews [15] address failure physics without linking it to converter selection; and recent technology-specific overviews [9, 12] treat GaN integration or EMC-oriented gate driving in isolation. A structured analysis that, within the specific context of high-frequency DC-DC converters, simultaneously addresses the following dimensions: (i) a silicon-referenced, normalized multi-parameter comparison matrix; (ii) topology-specific performance mapping; (iii) EMI spectral characterization across both materials; and (iv) unified reliability physics, has not, to the authors' knowledge, been systematically consolidated in a single decision-oriented framework. Table 1 positions the present review relative to representative prior reviews along these four dimensions.

Table 1 Positioning of this review relative to representative prior reviews of WBG power devices

Review	Normalized multi-metric matrix	Topology–performance mapping	EMI spectral comparison	Reliability physics	HF DC-DC converter focus
Millán et al. [4] (2014)	No	Partial	No	Partial	No
Castellazzi et al. [15] (2016)	No	No	No	Yes	No
She et al. [17] (2021), SiC-focused	No	Yes	No	Partial	Partial
Medinceanu et al. [9] (2026), GaN-focused	No	Yes	Partial	Partial	Yes
Wu et al. [12] (2026), EMC-focused	No	No	Yes	No	Yes
This review	Yes	Yes	Yes	Yes	Yes

Note: "Partial" denotes that the dimension is discussed qualitatively but not developed into a comparative SiC-versus-GaN analysis for high-frequency DC-DC converters.

Accordingly, this review is guided by four explicit research questions:

RQ1: How do the intrinsic material properties of SiC and GaN translate into converter-level performance metrics under defined voltage, frequency, and thermal conditions?

RQ2: Within which voltage–frequency–power regions does each technology demonstrate a verifiable advantage, and where do the technologies overlap?

RQ3: How do EMI generation, gate-driving, and thermal-packaging constraints modify device selection at the system level?

RQ4: Which reliability degradation mechanisms dominate under high-frequency DC-DC operating stress, and how are they mitigated?

The added value of the framework over a thematic synthesis is that it organizes the surveyed evidence into directly comparable, application-weighted criteria intended to support engineering technology-selection decisions, rather than presenting the SiC and GaN literatures in parallel.

1.2 Objectives and organization

The objectives of this review are fourfold: (i) to characterize the fundamental material properties of SiC and GaN with direct linkage to DC-DC converter performance; (ii) to construct a normalized comparative analysis framework enabling quantitative technology selection; (iii) to analyze system-level challenges in EMI management, gate driving, and thermal packaging; and (iv) to delineate future research directions for WBG technology maturation.

The remainder of this paper is organized as follows: Section 2 details the systematic literature evaluation methodology; Section 3 presents fundamental material physics; Section 4 introduces the comparative analysis framework; Section 5 maps converter topologies and application domains; Section 6 addresses system-level challenges; Section 7 discusses reliability physics; Section 8 identifies future directions; Section 9 presents conclusions.

2. Systematic Literature Evaluation Methodology

A structured literature evaluation was conducted targeting peer-reviewed publications, industry technical reports, and registered patents within the 2021–2026 timeframe. The review prioritizes studies presenting quantitative experimental validation of SiC and GaN device performance in high-frequency DC-DC converter applications. Databases utilized include IEEE Xplore, ScienceDirect, MDPI Open Access, and relevant IEEE conference proceedings, supplemented by patent analytics platforms. Searches combined the keyword groups (“SiC” OR “silicon carbide” OR “GaN” OR “gallium nitride” OR “wide bandgap”) AND (“DC-DC converter” OR “high-frequency” OR “switching frequency”) AND (“efficiency” OR “EMI” OR “reliability” OR “packaging”), applied to titles, abstracts, and keywords. Records were screened in two stages: title/abstract screening against the criteria of Section 2.1, followed by full-text assessment in which each retained study was checked for explicit reporting of the test conditions underlying its headline performance figures.

The final evidence base comprises the 22 sources cited in this review. Of this, 11 were published in 2021–2026 and constitute the core comparative dataset, while 11 earlier works [4-5, 7, 10-11, 15-16, 18-19, 21-22] provide foundational device physics and EMC context. Study quality was assessed by favoring peer-reviewed experimental work with hardware prototypes; manufacturer application material [1] was retained only for device-level parameter definitions and was not used as converter-level performance evidence.

2.1 Inclusion and exclusion criteria

Inclusion criteria required studies to: (i) present quantitative experimental or validated simulation results; (ii) explicitly address high-frequency operation (above 20 kHz); (iii) evaluate non-silicon primary switching devices; and (iv) be published within the defined five-year window. Excluded from the core comparative analysis were purely theoretical studies without

physical prototyping, grid-infrastructure studies below 10 kHz, and silicon-only investigations unless serving as explicit performance baselines.

2.2 Performance metric extraction protocol

To enable standardized cross-study comparison, a normalized metric extraction protocol was applied to all included studies. Each study was assessed against a common set of eight primary performance indicators: peak conversion efficiency (η), operating switching frequency (f_{SW}), voltage blocking class (V_2), conducted EMI frequency ceiling (f_E^{MI}), junction temperature headroom (ΔT_j), specific on-resistance ($R_{DS(on)}$), reverse recovery charge (Q_{rr}), and reported qualification standard. Where studies reported multiple operating points, values corresponding to the optimal efficiency or frequency condition were selected for the primary comparison. This extraction protocol forms the evidence base for the comparative analysis framework presented in Section 4.

It is acknowledged that extracting best-case operating points introduces a performance-selection bias, because peak efficiency is reached at different load fractions and topologies for different devices. Two safeguards are therefore applied: (i) all extracted converter-level figures are reported in Table 5 together with their topology, switching frequency, and rated conditions so that they are interpreted as reported best-case values rather than general technology limits; and (ii) cross-material comparisons are emphasized only for rows in which Si, SiC, and GaN devices were benchmarked within the same converter and test setup [5-6]. A further limitation is that intermediate screening counts (records identified, duplicates removed, records excluded per criterion) were not archived during the search and therefore a full PRISMA accounting cannot be reconstructed retrospectively; the inclusion criteria, search strings, and final corpus composition reported above are provided to make the evidence base traceable.

3. Fundamental Material Physics and Electro-Thermal Characteristics

3.1 Bandgap energy and thermal stability

A semiconductor's bandgap energy (E_S) defines the minimum energy required to promote a valence electron into the conduction band, directly governing both leakage current behavior and maximum operating temperature. Silicon possesses a narrow bandgap of approximately 1.1 eV, rendering it susceptible to thermally generated leakage currents at modest junction temperatures, effectively restricting maximum operating temperatures to approximately 150℃ [4]. In contrast, 4H-SiC features a bandgap of 3.26 eV and GaN 3.4 eV—approximately three times that of silicon—fundamentally suppressing thermally induced carrier generation by many orders of magnitude and enabling reliable operation at junction temperatures exceeding 200℃ [3-4].

3.2 Critical electric field and specific on-resistance

The critical electric field (Ec) is the maximum electric field intensity a semiconductor can sustain before avalanche breakdown initiates. SiC and GaN possess critical fields of 3.0 MV/cm and 3.3 MV/cm, respectively, approximately ten times the 0.3 MV/cm limit of silicon [4]. This tenfold advantage enables a fundamental geometric compression of the device drift region for any given voltage blocking requirement, described by the theoretical relationship for specific on-resistance:

$$R_{DS(on)} \propto \frac{V_B^{\,2}}{\mu_n \cdot \varepsilon_s \cdot E_c^{\,3}} \tag{1}$$

where V_B is the breakdown voltage, μ_n is the electron mobility, and ε_s is the dielectric permittivity of the semiconductor material. Because Ec appears as a cubic term, the tenfold advantage of WBG materials over silicon translates into a theoretical three-orders-of-magnitude reduction in $R_{DS(on)}$ for equivalent voltage ratings, fundamentally altering the conduction loss profile of high-voltage converters [3].

3.3 Carrier mobility and architectural divergence

Carrier mobility determines switching speed and conduction efficiency. SiC bulk electron mobility is approximately 900 $cm^2/V \cdot s$ at room temperature—lower than silicon's 1400 $cm^2/V \cdot s$, yet SiC's superior Ec compensates through geometric scaling. SiC power devices are therefore predominantly fabricated in a vertical MOSFET architecture, utilizing the full bulk semiconductor volume to distribute both current flow and electric field stress [4]. GaN's defining structural advantage originates at the AlGaN/GaN heterojunction interface [4]. Spontaneous and piezoelectric polarization mismatch at this interface induces a 2DEG, a quantum-confined sheet of electrons experiencing negligible ionized impurity scattering. The resultant electron mobility within the 2DEG channel approaches 2000 $cm^2/V \cdot s$ at 300 K [4], granting GaN lateral HEMT devices switching agility unmatched by any bulk semiconductor structure [4]. This lateral architecture, however, constrains commercial GaN devices to sub-650 V applications [2]. Fig. 1 illustrates the fundamental architectural distinction between vertical SiC MOSFET structures and lateral GaN HEMT devices, highlighting the differing current flow paths and electric field distributions that define their application domains.

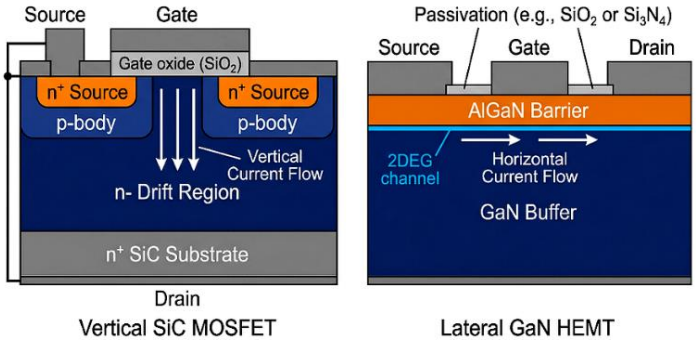

Fig. 1 Cross-sectional architecture of a vertical SiC MOSFET and a lateral GaN HEMT based on device structures in [4]

3.4 Thermal conductivity comparison

Thermal conductivity (λ) governs a device's ability to transfer heat from the semiconductor junction to the package. SiC is a bulk crystal with $\lambda \approx 370$ W/m·K—nearly 2.5 times that of silicon (≈ 150 W/m·K)—and vastly superior to standard GaN-on-Si implementations (≈ 130 W/m·K) [4]. This thermal superiority enables SiC devices to sustain extremely high power densities without reaching thermal failure thresholds, firmly establishing an advantage in multi-kilowatt continuous-duty applications such as EV traction inverters and grid-scale transformers [2]. Lateral GaN devices grown on silicon substrates (GaN-on-Si) face a compound thermal challenge: the inferior substrate conductivity creates a thermal bottleneck beneath the nanometer-scale 2DEG channel. Advanced composite substrates such as GaN-on-SiC partially resolve this by combining GaN's mobility advantage with SiC's thermal spreading capability, though at a substantial cost premium [4]. Table 2 summarizes the fundamental electro-thermal, electrical, and structural material properties of silicon, 4H-SiC, and GaN power semiconductor technologies relevant to high-frequency DC-DC converter applications.

Table 2 Fundamental material properties of Si, 4H-SiC, and GaN power semiconductors

	Material property	Si	4H-SiC	GaN (HEMT)
1	Bandgap energy, Eg (eV) [3]	1.1	3.26	3.4
2	Critical electric field, Ec (MV/cm) [4]	0.3	3.0	3.3
3	Electron mobility, μe ($cm^2/V \cdot s$) [4]	1400	900	~2000 (2DEG)
4	Thermal conductivity, λ (W/m·K) [4]	150	~370	~130 (on Si)
5	Max. Operating temperature (℃) [3]	~150	>200	>200
6	Reverse recovery charge (Qrr)	Extremely high	Very low	Zero (majority carrier)
7	Dominant architecture [4]	Vertical MOSFET/IGBT	Vertical MOSFET/JFET	Lateral HEMT
8	Commercial voltage range [4]	Up to 1700 V	600 V – 10 kV	Sub-650 V

Note: rows 1-4 are intrinsic material properties; rows 5-8 are device-, package-, and market-level characteristics; data compiled from [3-4].

The comparative electro-thermal and electrical performance characteristics of Si, SiC, and GaN summarized in Table 2 are further visualized in the radar comparison presented in Fig. 2. The radar plot normalizes each axis linearly to the maximum value among the three materials for the corresponding property; the switching-speed and maximum-temperature axes use representative device-class values from Table 2. Under this normalization, the bandgap axis places 4H-SiC (3.26 eV, score 0.96) almost coincident with GaN (3.4 eV, score 1.00), correctly reflecting their near-identical bandgap energies. These intrinsic properties map onto converter-level behavior as follows: bandgap and thermal conductivity bound the sustainable junction temperature and hence continuous power at a given cooling effort; critical field sets the achievable blocking voltage and specific on-resistance (conduction loss); and channel mobility together with gate and output charge governs switching loss and therefore the practical switching-frequency ceiling for a given topology. Sections 4 and 5 quantify these linkages under defined voltage, frequency, and topology conditions.

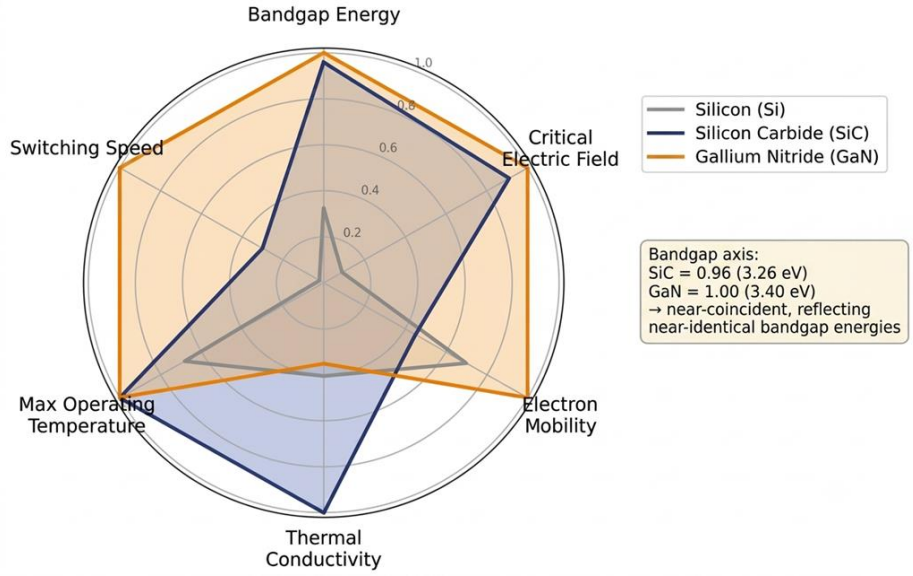

Fig. 2 Normalized material property comparison of Si, 4H-SiC, and GaN [3-4]

4. Comparative Analysis Framework

A standardized comparative analysis framework is introduced to enable objective, multi-dimensional evaluation of SiC and GaN technologies beyond single-metric comparisons. The framework consists of three interconnected components: (i) a normalized performance metric matrix; (ii) a frequency-voltage domain map defining the optimal territory for each device type; and (iii) a topology-performance matrix correlating converter architectures with empirically validated efficiency data.

4.1 Normalized performance metric matrix

Eight primary performance indicators are extracted from the surveyed literature and normalized against silicon baseline values, permitting direct cross-material comparison on a unified dimensionless scale. Let P^I denote the normalized performance score for indicator i, defined as:

$$P^I = \frac{x^I_{\mathrm{WBG}} - x^I_{\mathrm{Si}}}{x^I_{\mathrm{Si}}} \times 100 \tag{2}$$

where x^I, WBG is the WBG device metric value and x^I, Si is the silicon reference value for the same indicator. A positive score indicates an advantage of the WBG device over silicon, whereas a negative score indicates a relative disadvantage. Table 3 presents a normalized comparative performance matrix highlighting the relative advantages and limitations of SiC and GaN devices with respect to conventional silicon power semiconductors.

Three clarifications govern the interpretation of Table 3. First, the indicators belong to different levels of abstraction. Bandgap-derived voltage class and thermal conductivity are material/device-level quantities, whereas peak efficiency, switching frequency, EMI ceiling, and cost index are converter- and market-level quantities that depend on topology, package, layout, and operating point. The converter-level entries are therefore reported as the best values observed in the surveyed prototypes (traceable to the per-row citations and to Table 5) rather than as universal technology constants. Second, where the literature reports a spread, ranges are given (e.g., the cost index of 2.5–3.5 × for SiC and 2.0–4.0 × for GaN) to convey uncertainty. Single-valued entries should be read with an estimated uncertainty of at least one reporting step, since they originate from heterogeneous test conditions. Third, for decision-making the matrix is intended to be used with application-specific weighting. For a sub-650 V, density-driven design, the frequency, gate-charge, and reverse-recovery rows dominate the selection. In contrast, for an 800 V class, thermally constrained design, the voltage-class and thermal-conductivity rows dominate, as elaborated in the domain mapping of Section 4.2 and Table 4.

Table 3 Normalized performance comparison matrix of SiC and GaN vs. silicon baseline

Performance indicator	Si baseline	4H-SiC	GaN (HEMT)	Comparative interpretation
Peak efficiency η (%)	94.5	98.2	98.5	GaN marginally higher (topology-dependent)
Max. switching frequency [5]	20 kHz	300 kHz	>1 MHz	GaN strongly superior
Voltage blocking class [4]	1700 V	10 kV	<650 V	SiC strongly superior
Thermal conductivity (W/m·K) [4]	150	~370	~130 (on Si)	SiC strongly superior
Reverse recovery charge (Q_{rr}) [4]	Very high	Very low	Zero	GaN strongly superior
Gate charge figure of merit, $Q_g \cdot R_{DS(on)}$ (nC·Ω) [1]	~4	~2	<1	GaN strongly superior
EMI conducted emissions ceiling [1]	~10 MHz	~30 MHz	~400 MHz	SiC preferred (narrower EMI spectrum)
Relative component cost index [4]	1.0 (ref.)	2.5–3.5 ×	2.0–4.0 ×	Comparable (volume-dependent)

Note: converter-level rows report best-case values under the conditions of the cited studies; see Table 5 for the underlying operating contexts.

4.2 Frequency-voltage domain map

The confluence of gate charge, reverse recovery performance, and thermal conductivity defines clearly delineated optimal operating territories for each material class. These boundaries emerge from the fundamental trade-off between switching loss (which scales with frequency) and conduction loss (which scales with current and on-resistance). The theoretical efficiency crossover frequency, fc, at which GaN's lower switching losses begin to outweigh SiC's lower conduction losses in equivalent voltage class devices, can be approximated as:

$$f_c = \frac{\left(R_{DS(on),SiC} - R_{DS(on),GaN}\right) \times I_s^{oa\,2}}{E_{sw,SiC} - E_{sw,GaN}} \tag{3}$$

where I_s^{oa} is the rms output current, and E_{sw} represents the total switching energy per cycle for each device. Empirical data from boost converter benchmarks operating across 50 kHz to 5 MHz confirm that GaN devices achieve consistent efficiency leadership beyond approximately 100 kHz at voltage levels below 400 V [6]. SiC maintains a conduction efficiency advantage at voltages above 800 V across the 20–300 kHz range due to its superior thermal conductivity, enabling higher current densities without thermal throttling [2, 7]. The resulting frequency-voltage operating boundaries for silicon, SiC, and GaN devices are summarized in Fig. 3.

It must be emphasized that Fig. 3 is a first-order visualization: the voltage–frequency plane captures only two of the variables that determine device choice, which additionally depends on power level and current rating, converter topology, cooling strategy, package parasitics, EMI constraints, and qualification requirements. The map therefore includes an explicit

overlap region, approximately spanning 400–800 V and 100–300 kHz. In this region, 650 V GaN HEMTs, SiC MOSFETs, or hybrid SiC/GaN solutions may all be viable. The final selection is governed by these system-level priorities rather than by voltage and frequency alone.

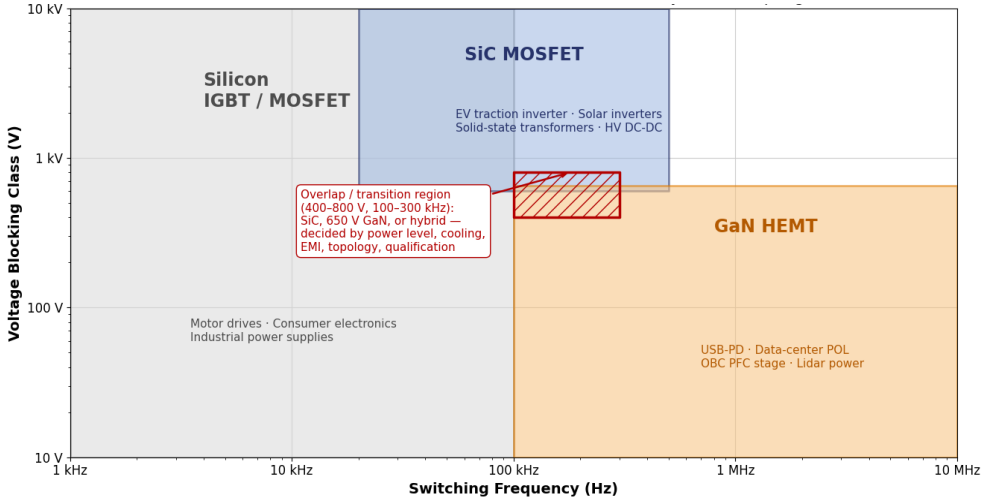

Fig. 3 Frequency-voltage domain map for Si, SiC, and GaN devices, highlighting the transition overlap region [2, 4, 6-7]

Three distinct operational frequency bands emerge from this analysis: silicon IGBTs are constrained to the 1–20 kHz band; SiC MOSFETs occupy the 20 kHz to approximately 300 kHz band; and GaN HEMTs demonstrate practical operation from 100 kHz to well beyond 1 MHz [4]. Recent investigations have explored application-specific deployment of SiC and GaN devices across automotive, industrial, aerospace, and data-center converter systems [4-5, 7]. Recent modulation and converter benchmark studies further evaluated SiC and GaN switching performance under advanced PWM and sigma-delta control strategies [8]. Emerging monolithic GaN converter platforms and ultra-high-density point-of-load architectures have also attracted significant research interest [9].

Recent EMC investigations and advanced PCB optimization studies have highlighted the growing importance of parasitic inductance control and EMI-aware converter design methodologies in WBG systems [10-12]. Advanced packaging structures, reliability qualification methods, and trench-gate SiC device architectures continue to improve the thermal and operational robustness of high-power WBG converters [13-15]. GaN-on-Si integration technologies, high-voltage SiC converter applications, and foundational AlGaN/GaN HEMT operating principles have also been extensively investigated for next-generation power electronics systems [16-18]. Recent studies additionally examined SiC body diode reliability mechanisms, automotive GaN device progress, and the broader system-level advantages of WBG power electronics in compact converter platforms [19-22]. Table 4 summarizes the strategic application domains of SiC and GaN technologies according to voltage class, operating frequency range, and converter requirements.

Table 4 Strategic application domain mapping by voltage class, frequency, and preferred WBG technology

Application domain	Voltage class	Frequency range	Preferred technology (context-dependent)	Primary justification
Consumer electronics / USB-PD [4]	< 100 V	300 kHz – 1 MHz+	GaN HEMT	Zero Q_{rr}, low Qg, ultra-compact passives
Data center POL converters [9]	48 V → 1 V	1 MHz – 5 MHz	GaN IC	Monolithic integration, 123.3 kW/L density
EV OBCs [7]	400 V – 800 V	100 kHz – 300 kHz	Stage-dependent: GaN (totem-pole PFC, ≤650 V); SiC (800 V isolated DC-DC stage)	GaN efficiency in the PFC stage; SiC voltage margin and thermal robustness at 800 V
EV traction inverters [17]	600 V – 1200 V	20 kHz – 100 kHz	SiC MOSFET	Bulk thermal conductivity, avalanche ruggedness

Table 4 Strategic application domain mapping by voltage class, frequency, and preferred WBG technology (continued)

Application domain	Voltage class	Frequency range	Preferred technology (context-dependent)	Primary justification
Industrial welding supplies [5]	400 V – 800 V	100 kHz – 200 kHz	GaN HEMT (≤650 V bus) / SiC (800 V class)	98.5% peak efficiency and 45% heatsink volume reduction at 600 V class [5]; SiC preferred near 800 V for voltage margin
Grid-tied solid-state transformers [21]	> 1200 V	10 kHz – 50 kHz	SiC MOSFET/JFET	Exceptional breakdown field, thermal cycling stability
5G RF / Aerospace power [16]	28 V – 50 V	GHz (RF power-amplifier domain; included for completeness)	GaN-on-SiC	2DEG mobility + SiC thermal substrate integration

Note: recommendations are indicative, stage- and condition-dependent; overlap regions correspond to Fig. 3.

5. High-Frequency Switching Performance and Converter Topology Analysis

5.1 Switching dynamics and gate charge optimization

The ultra-high 2DEG electron mobility of GaN HEMTs translates directly into unparalleled switching speed. GaN devices exhibit a gate-charge figure of merit ($Q^k \cdot R_{DS(on)}$) below 1 nC·Ω, compared to approximately 4 nC·Ω for an equivalent-rating silicon MOSFET [1]. This difference reflects the far smaller gate charge required to fully enhance the conduction channel for a given on-resistance class. This reduction in Q^k directly decreases the power dissipated within the gate driver circuit per switching cycle:

$$P_{ate}^{k} = Q^{k} \times V_{s}^{k} \times f_{s}^{W} \tag{4}$$

where V_s^k is the gate drive voltage and, f_s^w is the switching frequency. With Q^k four times lower than silicon, GaN devices can operate at MHz-range frequencies while maintaining gate drive power consumption within practical thermal bounds. Furthermore, GaN's highly nonlinear output capacitance (C_{OSS}) ensures that switching energy (E_{OSS}) remains substantially constant across the drain voltage range, a critical advantage for maintaining efficiency across varying load conditions [1].

5.2 Reverse recovery loss elimination

Perhaps the most electrically consequential distinction between GaN and both SiC and silicon concerns reverse recovery behavior. In continuous conduction mode (CCM) half-bridge topologies, such as synchronous buck and boost converters, the low-side switch body diode conducts freewheeling current during dead-time intervals. At subsequent high-side turn-on, stored minority carrier charge in silicon diodes must be forcibly extracted, generating a reverse recovery current spike. The associated switching loss is given by:

$$E_{\mathrm{rr}} = \frac{1}{2} \times Q_{\mathrm{rr}} \times V_{\mathrm{DC}} \tag{5}$$

where V_{DC} is the DC bus voltage. The GaN HEMT is a pure majority-carrier device that conducts reverse current through the 2DEG channel rather than a parasitic p-n junction. Consequently, it exhibits absolute zero reverse recovery charge ($Q_{rr} = 0$), eliminating this loss component entirely [1]. SiC MOSFETs do possess a parasitic body diode with a finite Q_{rr}, though this is several orders of magnitude lower than that of silicon equivalents, permitting high-frequency operation in applications where GaN's voltage limitation is prohibitive [1].

5.3 Hard-switched converter topology performance

Empirical evaluation of hard-switched high-gain boost converters operating across 50 kHz to 5 MHz confirms GaN's efficiency leadership. At 200 kHz and a 0.5 duty cycle, GaN-based converters achieved a peak conversion efficiency of 94%, measurably exceeding SiC (93.67%) and Si (93.54%) [6]. More notably, GaN maintained high continuous voltage gains up to 6.33 at a 0.7 duty cycle without thermal saturation, demonstrating superior capacity for extreme duty ratio operation under hard-switching conditions. At the system level, an enhancement-mode GaN FET buck converter prototype for EV power modules operated efficiently at 350 kHz, whereas the silicon baseline required restriction to 100 kHz to prevent thermal destruction. This resulted in an overall system efficiency improvement from 93.25% to 96.61% alongside a significant volumetric reduction in passive inductors and capacitors [3]. The comparative high-frequency switching behavior and topology-level performance trends of SiC and GaN devices are illustrated in Fig. 4.

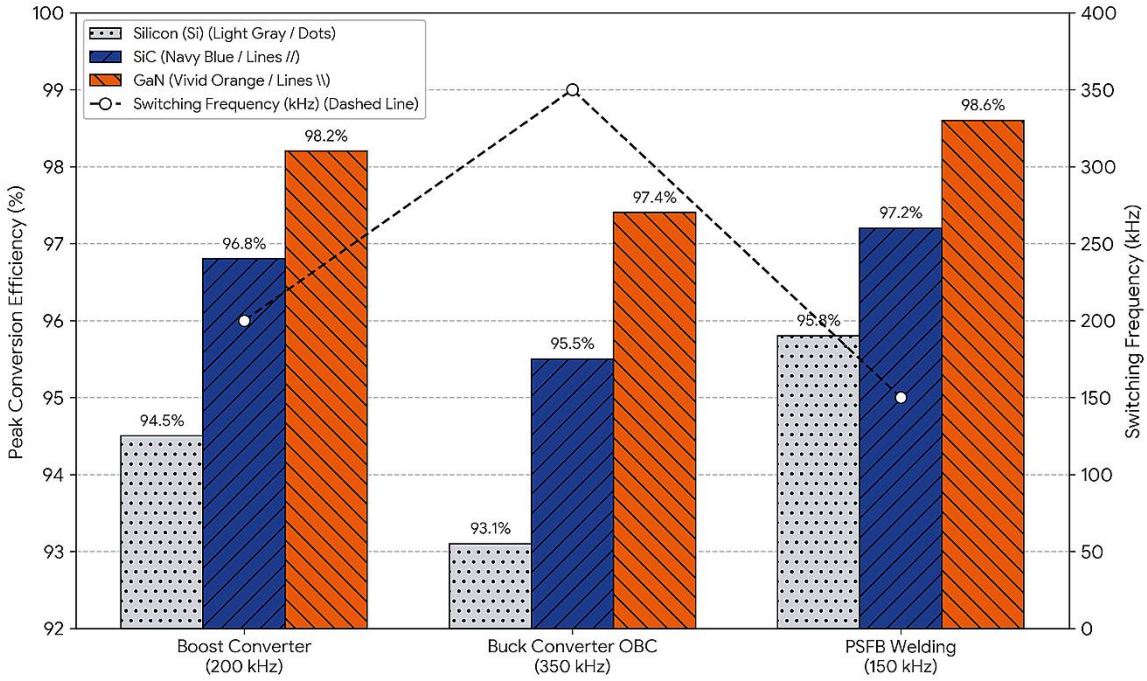

Fig. 4 Comparative switching performance of SiC and GaN converter topologies [3, 5, 6]

5.4 Soft-switched and resonant topology performance

Soft-switching topologies, including inductor inductor capacitor (LLC) resonant converters, dual active bridge (DAB), and phase-shifted full-bridge (PSFB) utilize reactive tank circuits to enforce zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions, dramatically reducing switching losses. In a 10 kW PSFB DC-DC converter prototype designed for industrial welding power supplies, GaN HEMTs enabled stable operation above 150 kHz—a 60% frequency increase over the silicon IGBT baseline—facilitating a 45% reduction in heatsink volume and enabling compact planar transformer integration. Under these conditions, GaN recorded a peak efficiency of 98.5%, marginally outperforming SiC (98.2%) and vastly surpassing the Si IGBT baseline (94.5%) [5].

In LLC resonant converters targeting 1 kV / 3 kW outputs, GaN inherently provides lower total switching losses, enabling peak efficiencies approaching 99.6% at operating frequencies exceeding 1 MHz [4]. However, SiC MOSFETs demonstrate more predictable ZVS behavior under variable load conditions due to their larger, more linear output capacitance profiles. The highly nonlinear C_{OSS} characteristic of lateral GaN HEMTs complicates ZVS range optimization across wide load ranges and requires more sophisticated resonant tank design methodologies [4]. Table 5 presents experimentally reported converter performance metrics across representative hard-switched and resonant converter topologies employing SiC and GaN devices.

Table 5 Empirical performance comparison across converter topologies and WBG materials (2021–2026)

Topology / Application	Si η (%)	SiC η (%)	GaN η (%)	F_{SW} (kHz)	GaN voltage class (V) / reported conditions
High-gain boost converter [6]	93.54	93.67	94.00	200	400; 0.5 duty cycle; hard-switched; power n.r.
EV buck converter (OBC) [3]	93.25	N/A	96.61	350	400; 48 V-bus EV power module; power n.r.
PSFB welding converter [5]	94.50	98.20	98.50	>150	600; 10 kW rated; planar transformer
LLC resonant OBC / Server [4]	N/A	~98.5	99.60	>1000	650; 1 kV / 3 kW output; ZVS
SiC / GaN VSC (SVPWM vs H-ΣΔ) [8]	N/A	~98.74	>99.0	200	650; modulation-dependent; power n.r.
Monolithic GaN POL IC [9]	N/A	N/A	>98.0	25,000	100; 48 V→1 V POL; 123.3 kW/L

Note: all η values are peak efficiencies as reported under each study's own test conditions; row-level Si/SiC/GaN comparisons are internally consistent within each cited setup, but cross-row comparison and broad superiority claims are not supported because input/output voltage, rated power, load condition, cooling method, device rating, and package differ between studies; "n.r." = not reported

6. System-Level Challenges in High-Frequency WBG Design

6.1 EMI and parasitic inductance management

The primary adverse consequence of ultra-fast WBG switching transitions is the generation of severe EMI. When voltage slew rates (dv/dt) exceed 50 V/ns, and current slew rates (di/dt) surpass 10 A/ns, the resulting high-frequency energy couples capacitively through parasitic heatsink paths and inductively through PCB traces. This coupling generates common-mode (CM) and differential-mode (DM) conducted emissions that can violate regulatory standards such as International Special Committee on Radio Interference (CISPR) 25 [10]. A critical distinction exists between the EMI spectra of SiC and GaN devices. Inverter configurations utilizing SiC MOSFETs typically exhibit conducted emissions concentrated below 30 MHz, aligning with existing EMC filter design infrastructure. GaN HEMTs, with their near-instantaneous voltage edge rates, generate broadband conducted noise extending to approximately 400 MHz — a frequency range thirteen times wider than SiC and fully two orders of magnitude beyond silicon baselines [1]. This spectral difference fundamentally necessitates entirely distinct multi-stage filter architectures for GaN designs.

It is stressed that the quoted spectral ceilings, dv/dt figures, false turn-on susceptibility, and spread-spectrum attenuation values reported in this section are strongly dependent on PCB layout, package parasitics, gate-driver design, bus voltage, and the applicable test standard; they should therefore be treated as system-level decision criteria for a specific design context rather than as general device-level attributes. The comparative EMI spectral distribution characteristics of SiC and GaN devices are illustrated in Fig. 5.

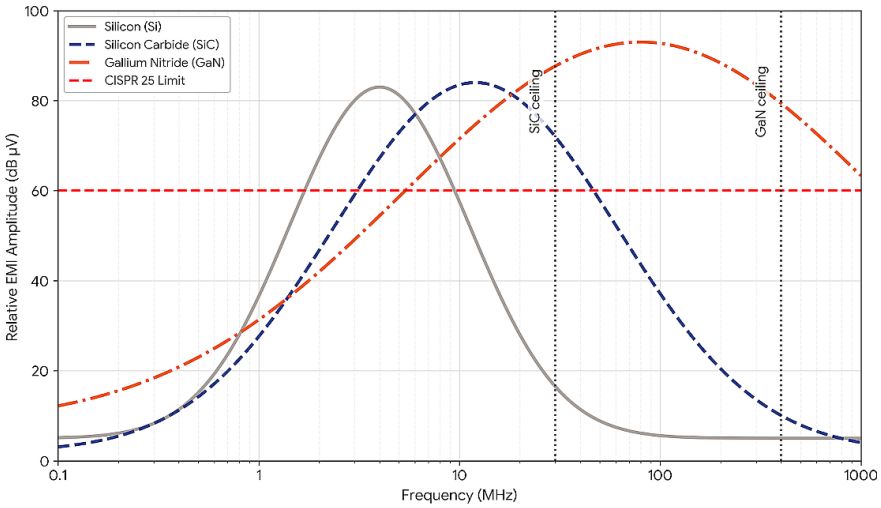

Fig. 5 Conducted EMI emission spectra for Silicon, SiC, and GaN devices [10-12]

At the PCB level, GaN HEMTs' low gate threshold voltage ($V_t^h \approx 1.5$ V) and narrow maximum gate voltage margin create extreme susceptibility to false turn-on events. During a complementary switch's turn-on, the rapid dv/dt transient drives a displacement current through the parasitic Miller capacitance (C_{gd}). Even a few nanohenries of parasitic gate loop inductance convert this current into a gate voltage spike that can trigger catastrophic shoot-through [3]. Electromagnetic simulation results demonstrate that optimized multilayer PCB routing with strategic DC-link capacitor placement can reduce total commutation loop inductance by 40%, successfully preserving switching performance while suppressing resonant ringing [11].

6.2 Advanced gate driving and EMC collaborative (CO)-design

Traditional EMI mitigation through indiscriminate gate resistance (R^g) increase is counterproductive for WBG devices, increasing switching losses by 12–15% and effectively eliminating the efficiency advantage of WBG selection [12]. Modern adaptive gate drivers must instead operate as intelligent high-bandwidth analog actuators managing the switching trajectory to suppress EMI at the source. For high-frequency noise suppression above 50 MHz, segmented gate drivers, current-source drivers (CSD), and negative-bias off-state clamping circuits are employed to control the Miller plateau and inject anti-phase compensation currents during nanosecond switching edges [12]. For low-frequency conducted emissions below 50 MHz, continuous random spread-spectrum modulation (C-RSSM) using analog Markov-chain chaotic signal generators continuously randomizes the switching frequency, preventing harmonic energy concentration at fundamental multiples. C-RSSM achieves up to 35 dBμV of EMI attenuation relative to fixed-frequency operation [12]. The principal challenge of C-RSSM is that continuous frequency randomization severely disrupts standard PWM feedback control loops. Instantaneous duty-cycle tracking (ITR) feedback paths resolve this by synchronously adjusting the transistor on-time on a cycle-by-cycle basis [12].

6.3 Thermal management and advanced packaging

The extreme localized power densities generated within nanometer-scale WBG semiconductor dies transform thermal management from a secondary design consideration into the primary constraint on continuous output power. GaN-on-Si substrates face severe thermal choke points immediately beneath the 2DEG channel, where localized thermal flux densities can reach values that cause premature thermal failure despite modest total dissipation [2]. Traditional wire-bonded packaging introduces prohibitive parasitic inductances and represents the primary thermo-mechanical failure site under repetitive power cycling stress [13]. The industry is transitioning toward wire-bondless packaging utilizing silver sintering for die attachment to direct bonded copper (DBC) or active metal brazed (AMB) ceramic substrates. Double-sided cooling (DSC) structures sandwich the semiconductor die between two thermally conductive planes, thereby lowering the effective junction-to-case thermal resistance (θjc) by providing two simultaneous heat extraction pathways [2]. The thermal evolution from conventional packaging toward advanced double-sided cooling and low-inductance module structures is illustrated in Fig. 6.

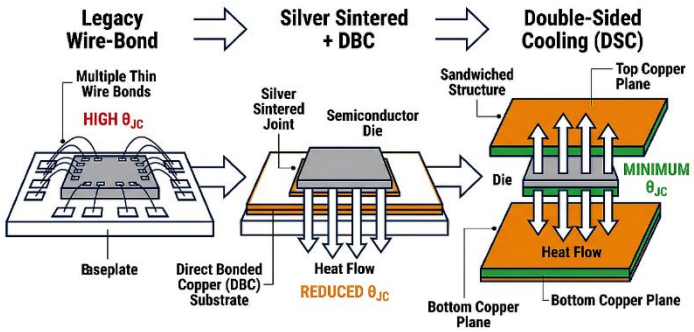

Fig. 6 Evolution of power semiconductor packaging and thermal management stages [2, 13]

For SiC specifically, monolithic integration of a unipolar diode within the trench-gate MOSFET structure bypasses the intrinsic lossy body diode. This integration suppresses the hole injection that drives basal plane dislocation (BPD) propagation during reverse conduction. Device simulations of this architecture report reduced reverse conduction voltage and reverse

recovery charge together with lower switching losses, easing the thermal burden relative to discrete anti-parallel diode implementations [14]. Table 6 compares the principal EMI characteristics, parasitic sensitivity, and mitigation strategies associated with SiC and GaN converter implementations.

Table 6 EMI characteristics and mitigation strategies for SiC and GaN in high-frequency DC-DC converters

EMI parameter	SiC MOSFET	GaN HEMT	Mitigation strategy
Conducted emission ceiling [1]	~30 MHz	~400 MHz	Multi-stage LC + CM choke
Max. dv/dt (V/ns) [12]	10–30	>50	Segmented / current-source gate drivers
False turn-on susceptibility [3]	Low	High (Vth ≈ 1.5 V)	Negative gate bias, Kelvin source connections
PCB parasitic inductance sensitivity [11]	Moderate	Extreme	Multi-layer PCB; 40% inductance reduction achievable [11]
Spread-spectrum modulation benefit [12]	Moderate	High (35 dBμV) [12]	C-RSSM with ITR duty-cycle tracking
Applicable EMC standard [10]	CISPR 25 / 32	CISPR 25 / AEC-Q101	Digital pre-compliance simulation essential

Note: values are design- and test-condition-dependent; compiled from [7, 10-12].

7. Reliability Physics and Degradation Mechanisms

Device selection for high-frequency DC-DC converters cannot rest on efficiency and power density alone, because the two technologies fail through fundamentally different physical mechanisms and therefore demand different qualification strategies. SiC MOSFET degradation is dominated by gate oxide integrity and bipolar effects rooted in the SiO_2/SiC interface and the underlying crystal lattice, whereas GaN HEMT reliability is governed by charge trapping and threshold voltage instability within the AlGaN/GaN heterostructure. This section examines each failure landscape in turn and consolidates the comparison in Table 7.

7.1 SiC MOSFET failure mechanisms

The dominant reliability challenge for SiC MOSFETs originates at the SiO_2/SiC gate oxide interface. Lattice mismatch between the SiC crystal and the thermally grown silicon dioxide dielectric layer creates a significantly elevated density of interface trap states compared to Si/SiO_2 systems. Under sustained high electric fields and elevated junction temperatures, time-dependent dielectric breakdown (TDDB) accelerates through Fowler-Nordheim tunnelling mechanisms, ultimately precipitating hard gate oxide failure [15]. Accelerated lifetime testing following JEDEC qualification protocols reveals that the mean time to failure (MTTF) due to TDDB follows a Weibull distribution with a shape parameter strongly dependent on oxide field strength and operational temperature.

A secondary but critical SiC degradation mechanism involves BPDs—crystallographic defects inherent to the SiC epitaxial growth process. During third-quadrant body diode conduction, hole-electron recombination at BPD sites releases sufficient energy to propagate the dislocation through the crystal lattice [17], expanding into shockley-type stacking faults. Monolithic integration of a unipolar diode structure, which diverts reverse current away from the body p-n junction, is an effective topological strategy to suppress BPD propagation [14].

7.2 GaN HEMT failure mechanisms

GaN HEMTs exhibit a distinctly different failure physics landscape centered on charge trapping phenomena within the AlGaN/GaN HEMT architecture originally established in foundational GaN device studies [19]. During high-voltage off-state blocking, hot electrons can be injected into trap states within the carbon-doped GaN buffer layer, the AlGaN barrier layer, or the SiN^x surface passivation interface. Upon subsequent device turn-on, trapped charges physically repel 2DEG electrons beneath them, causing a temporary elevation in dynamic on-resistance—a phenomenon termed current collapse or dynamic

$R_{DS(on)}$ degradation [2]. In worst-case conditions, dynamic $R_{DS(on)}$ can increase by 50–300% over static values, severely impacting converter efficiency and thermal management assumptions.

Additionally, enhancement-mode p-GaN gate structures — the dominant architecture for commercially normally-off GaN HEMTs—exhibit susceptibility to threshold voltage (V_t^h) drift under sustained positive gate bias stress. Positive bias temperature instability (PBTI), driven by hole trapping at the p-GaN/AlGaN interface, causes a permanent V_t^h shift that complicates accurate lifetime degradation prediction and SPICE model validation across operating lifetime [2].

These mechanisms are excited by specific high-frequency DC-DC operating stresses: (i) sustained dv/dt above 50 V/ns elevates gate oxide field stress in SiC and drives off-state hot-electron trapping in GaN; (ii) dead-time third-quadrant conduction in CCM half-bridges activates SiC body diode BPD propagation; (iii) repetitive hard-switching cycles accelerate dynamic $R_{DS(on)}$ drift in GaN; and (iv) mission-profile thermal cycling stresses die-attach and CTE-mismatched interfaces in both technologies. Reliability assessment should therefore be performed against the converter's actual switching trajectory and mission profile rather than against static datasheet stress tests alone. Fig. 7 summarizes the principal degradation and reliability mechanisms affecting SiC MOSFETs and GaN HEMTs under high-frequency operational stress. Table 7 summarizes the dominant reliability degradation mechanisms, qualification considerations, and mitigation approaches for SiC MOSFETs and GaN HEMTs under high-frequency operating stress.

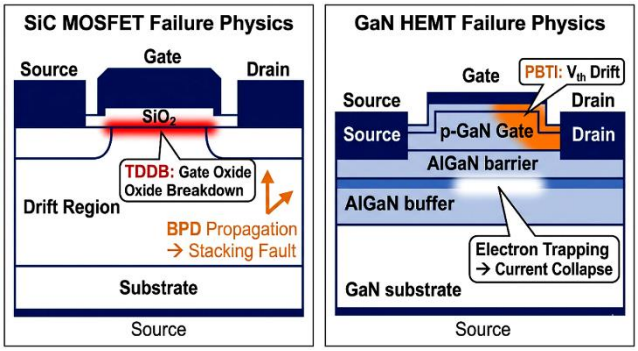

Fig. 7 Reliability degradation mechanism comparison based on [2, 14-15, 18-19]

Table 7 SiC MOSFET and GaN HEMT reliability under high-frequency stress based on [2, 13-15, 18-19]

Reliability parameter	SiC MOSFET	GaN HEMT
Primary failure mode [15]	Gate oxide TDDB (SiO_2/SiC interface traps)	Charge trapping / Dynamic $R_{DS(on)}$ degradation
Secondary failure mode [14]	BPD propagation	p-GaN gate Vth drift (PBTI)
Gate oxide reliability [15]	Moderate (SiO_2 lattice mismatch)	Superior (no SiO_2 interface)
Mitigation strategy [14]	Integrated unipolar diode; trench-gate structure	GaN-on-SiC substrate; optimized carbon doping profile
Qualification standard [15]	AEC-Q101; IEC 60747	AEC-Q101 (GaN addendum); JEDEC JEP180
thermal cycling Robustness [13]	High (bulk crystal, silver sintering)	Moderate (GaN-on-Si CTE mismatch concern)
Dominant HF DC-DC operating stressors	High dv/dt gate-oxide field stress; dead-time reverse (third-quadrant) conduction; thermal cycling of die attach	Off-state high-voltage blocking with fast dv/dt (hot-electron trapping); repetitive hard switching (dynamic $R_{DS(on)}$); CTE-mismatch thermal cycling

8. Emerging Research Gaps and Future Directions

The performance, EMC, thermal, and reliability limitations identified in Sections 5 through 7 define the boundaries of present WBG converter design and, in doing so, indicate where the most consequential research effort now lies. Four directions

emerge from the surveyed literature: (i) monolithic integration to eliminate the layout parasitics that constrain discrete GaN, (ii) virtual pre-compliance methods to replace iterative EMC prototyping, (iii) hybrid device configurations that combine SiC and GaN strengths within a single converter, and (iv) ultra-wide-bandgap materials that extend beyond the physical limits of both. Each is examined below with respect to its principal technical barrier.

8.1 Monolithic GaN integrated circuits

The extreme sensitivity of discrete GaN HEMTs to PCB layout parasitics is driving an accelerating industry paradigm shift toward monolithic integration. By co-fabricating the gate driver, diagnostic logic, protection circuits, and the primary power HEMT on a single continuous GaN substrate, parasitic gate loop inductance is effectively reduced to near zero [9]. Recent advancements have yielded monolithic GaN ICs demonstrating stable operation at 30 mΩ on-resistance with 25 MHz switching frequency [20]. A space-grade point-of-load converter built on this platform achieved an unprecedented power density of 123.3 kW/L [9].

The principal barrier to widespread deployment remains the astronomical cost of large-area, defect-free epitaxial GaN wafer growth. Continued progress in metal-organic chemical vapor deposition (MOCVD) equipment precision and wafer diameter scaling are the critical path items. Beyond cost, qualification of monolithic GaN ICs requires demonstration of thermal coupling limits between co-integrated driver and power stages and of long-term dynamic $R_{DS(on)}$ stability under application mission profiles; the near-term application relevance is concentrated in 48 V data-center and aerospace point-of-load conversion, where extreme density justifies the substrate cost.

8.2 EMC digital twins for pre-compliance validation

Traditional power electronics development—design, prototype fabrication, EMC testing, and iterative redesign—is fundamentally unsustainable for MHz-range WBG converters, where EMI spectral characteristics are exquisitely sensitive to millimeter-level PCB trace routing variations. A critical research gap exists for holistic, physics-based multi-domain simulation platforms termed EMC digital twins. These platforms must simultaneously and self-consistently resolve: (i) nonlinear semiconductor switching dynamics at nanosecond timescales; (ii) distributed three-dimensional parasitic electromagnetic networks at sub-millimeter spatial resolution; (iii) thermal heat flux evolution through package materials; and (iv) thermo-mechanical stress at solder joint interfaces [12].

The development and experimental validation of such EMC digital twins would enable pre-compliance certification against automotive standards such as CISPR 25 and ISO 26262 entirely within a virtual environment, dramatically compressing development cycle time. The principal technical barriers are the disparate timescales (nanosecond switching versus seconds-scale thermal transients) that defeat monolithic solvers and the scarcity of validated broadband (above 100 MHz) behavioral models for commercial WBG devices. Credible progress therefore requires published correlation studies between simulated and measured CISPR 25 spectra on identical hardware before digital-twin pre-compliance can be accepted by certification bodies.

8.3 Hybrid and cascode topologies

At the converter systems level, hybrid topologies strategically combining the complementary strengths of SiC and GaN are attracting substantial research interest. GaN/Si cascode configurations merge the normally-off gate drive simplicity of a mature low-voltage silicon MOSFET with the high-voltage blocking and switching speed of a normally-on GaN HEMT. The resulting composite device is simultaneously gate-drive compatible with existing silicon infrastructure and capable of WBG switching performance [4]. Research into series-stacked hybrid half-bridge configurations pairing SiC for the high-side switch with GaN for the low-side switch in asymmetric voltage bus topologies promises to extend GaN's efficiency advantage into the 650–1200 V application space currently monopolized by SiC.

Open barriers include dynamic voltage sharing and gate-timing coordination between dissimilar devices, fault protection of the normally-on GaN element in cascode stacks, and the absence of standardized qualification procedures for mixed-technology switches. Experimental validation in full-power prototypes with documented EMI and reliability data, rather than simulation-only studies, is required. Such validation is necessary before hybrid topologies can be recommended for the 800 V EV bus.

8.4 Ultra-wide-bandgap (UWBG) materials

The approaching physical limits of SiC and GaN are driving heavily funded fundamental research into UWBG semiconductor materials. Beta-gallium oxide (β-Ga_2O_3) features a bandgap of approximately 4.8 eV and a theoretical critical electric field of 8 MV/cm—more than double that of GaN—while synthetic single-crystal diamond exhibits a bandgap of 5.4 eV with theoretical thermal conductivity exceeding 2000 W/m·K [2]. If current epitaxial growth challenges are resolved, these materials promise power converter devices capable of blocking multi-kilovolt potentials at switching frequencies of tens of MHz with minimal active cooling infrastructure. Such capabilities could fundamentally redefining the boundaries of power density and conversion efficiency for future electrified systems. The decisive barriers are material-specific: β-Ga_2O_3 suffers from intrinsically low thermal conductivity (more than an order of magnitude below SiC) and the lack of practical p-type doping, which together constrain device architecture and heat extraction. In contrast, single-crystal diamond remains limited by wafer diameter, cost, and doping control. UWBG insertion into DC-DC conversion therefore presupposes validated thermal co-design solutions and kilovolt-class switching demonstrations under converter-representative dv/dt stress.

9. Discussion

The analysis presented in Sections 3 through 8 establishes that the selection between SiC and GaN for high-frequency DC-DC converter applications is fundamentally a multi-dimensional optimization problem, not a binary competition. The normalized comparative framework (Table 3) and domain mapping (Table 4) together confirm that each technology occupies a distinct, physics-justified application territory with minimal overlap. GaN's 2DEG electron mobility advantage, zero reverse recovery charge, and sub-1 nC·Ω gate-charge figure of merit establish a decisive switching-speed advantage in the sub-650 V domain. This translates into reported efficiency leadership across the surveyed hard-switched and resonant topologies at frequencies above 100 kHz, under the respective operating conditions documented in Table 5. The 45% heatsink volume reduction achieved in the PSFB prototype [5] directly quantifies the system-level value of GaN's frequency advantage in compact converter design.

However, GaN's thermal conductivity deficiency (~130 W/m·K on Si versus ~370 W/m·K for SiC bulk) imposes a ceiling on sustained high-current operation that is not compensated by superior switching performance at elevated power levels. This thermal boundary, combined with the 650 V commercial voltage limit, positions SiC as the preferred technology for EV traction inverters, grid-scale transformers, and high-power industrial converters under sustained high-current operating conditions. The system-level challenge that most fundamentally differentiates WBG design methodology from legacy silicon practice is EMI management. The 400 MHz noise ceiling of GaN (Table 6) requires filter architectures, gate driver circuits, and PCB layout disciplines that represent a complete engineering paradigm shift. As demonstrated by the C-RSSM technique achieving 35 dBμV attenuation [12], solutions exist but introduce considerable system complexity and cost that must be weighed against the efficiency and density benefits of GaN adoption.

From a reliability perspective, both materials present unique qualification challenges (Table 7) that require continued physics-of-failure modeling refinement. The resolution of GaN charge trapping and SiC gate oxide interface defect density through advanced epitaxial growth techniques and novel passivation materials constitutes the critical path for universal automotive-grade WBG deployment. Synthesizing Sections 3–7, device selection is jointly determined by five coupled criteria

rather than by any single metric: (i) the required blocking voltage and its margin fix the admissible technologies; (ii) the target switching frequency and topology determine whether GaN's switching-loss advantage is realizable; (iii) the thermal architecture and continuous current decide whether GaN-on-Si thermal limits or SiC's bulk conductivity dominate; (iv) the applicable EMC standard and layout discipline set the cost of exploiting fast edges; and (v) the qualification and mission-profile reliability requirements weight the residual degradation risks of each material. A defensible technology choice is the intersection of these constraints for a specific converter stage, which is why the framework of Section 4 attaches operating context to every comparative figure.

10. Conclusions

This comparative review has systematically analyzed SiC and GaN power semiconductor devices for high-frequency DC-DC converter applications through a structured multi-dimensional framework. The analysis encompasses material physics, normalized performance metrics, topology-specific empirical data, EMI characteristics, thermal management paradigms, and reliability physics. The following principal conclusions are drawn:

(1) GaN HEMTs demonstrate clear efficiency leadership in the surveyed prototypes (up to 98.5% in a 10 kW PSFB converter [5]) and superior switching frequency capability (100 kHz to >1 MHz) in sub-650 V converter applications, driven by zero reverse recovery charge, a sub-1 nC·Ω gate-charge figure of merit, and 2DEG electron mobility approaching 2000 $cm^2/V \cdot s$. Under these voltage, frequency, and cooling conditions, GaN is the best-suited technology for consumer electronics, data center POL converters, and the PFC stage of EV OBCs, provided that EMI mitigation and thermal limitations are addressed at the system level.

(2) SiC MOSFETs retain a decisive advantage in the high-voltage (>800 V), high-power domain [17]. These properties, including superior bulk thermal conductivity (~370 W/m·K), exceptional avalanche ruggedness, and validated reliability under automotive qualification standards establish SiC as the preferred technology for EV traction inverters, solid-state transformers, and megawatt-scale renewable energy inverters.

(3) System-level EMI management constitutes the most formidable practical challenge for GaN converter design. The 400 MHz conducted emission ceiling demands fundamentally new filter architectures, advanced gate driving strategies incorporating C-RSSM with ITR compensation, and rigorous multilayer PCB co-design achieving up to 40% parasitic inductance reduction.

(4) Advanced packaging technologies including silver sintering, double-sided cooling structures, and monolithic diode integration for SiC are essential enablers of the electro-thermal performance levels demonstrated in experimental studies. These technologies represent the critical path from laboratory efficiency to commercially qualified module reliability.

Future trajectories including monolithic GaN ICs (achieving 123.3 kW/L power density) [9], EMC digital twin simulation platforms, hybrid SiC/GaN converter topologies, and UWBG materials (β-Ga_2O_3, diamond). These technologies will further extend the performance boundaries of WBG power electronics over the next decade.

The overarching conclusion is that WBG power electronics demands a holistic, multi-physics CO-design philosophy that simultaneously optimizes semiconductor selection, converter topology, EMC compliance strategy, thermal architecture, and packaging technology. As this co-design methodology matures—supported by digital twin validation tools and advanced manufacturing processes—SiC and GaN will transition from novel technological differentiators to the foundational infrastructure of the global electrified energy economy.

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Conflicts of Interest

The authors declare no conflict of interest.

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