

A 20-GHz On-Chip Six-Port Reflectometer Using Simple Lumped Passive Devices and Bipolar Junction Transistors

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Abstract

This paper proposes an on-chip six-port reflectometer (SPR) fabricated in the 0.13- μm IBM BiCMOS-8HP technology. The SPR enjoys a compact circuit structure, with only four amplitude detectors as active devices, one resistive power divider, and one lumped phase shifter as passive devices. The power divider and phase shifter are responsible for manipulating the radio-frequency (RF) signals appropriately, whereas the detectors are responsible for sensing the processed signals. The chip area, which can be further reduced, is 1.25 mm in width and 1 mm in height. The SPR can perform in-situ measurement of reflection coefficients of devices under test (DUTs) and reduce testing costs of RF chips by using vector network analyzers (VNAs). The SPR demonstrates excellent performance in measuring the reflection coefficients of DUTs at around 20 GHz. The experimental results indicate that the maximum error of the measured reflection coefficients in absolute value is about -26 dB.

Keywords: On-chip measurement, six-port reflectometer, reflection coefficient, amplitude detector, vector network analyzer

1. Introduction

The idea of SPR [1] was proposed to perform the measurement of the reflection coefficient of a device-under-test (DUT). Since its first emergence, the concept of SPR measurement has been continually developed with time. The developments can be mainly categorized into two branches — the variations in the system or circuit implementations [2-6] and the advances in the calibration algorithms [7-14].

For the variations in circuit implementations, a compact structure substantially reducing the circuit complexity and facilitating the simplicity of realizing SPR in integrated circuits (ICs) was proposed in [3]. According to [3], the SPR can operate up to 3 GHz.

For the improvements in the calibration methods, [12] proposed a robust and economical algorithm that can complete the calibration of an SPR's core parameters with only five loads. These loads, also known as the sliding terminations, need to possess reflection coefficients of approximately equal magnitude but different phases. Compared to the previous work in [8], which requires nine loads for calibration, the costs of preparing the calibration standards are greatly reduced. Moreover, by combining the advantages from the former work [7, 10-11] with the new ideas that can help prevent ill-conditioned situations, the algorithm by [12] provides improved robustness in restoring an erroneous SPR to normal operation. Since process variations are ubiquitous, inevitable, and unpredictable variables in modern semiconductor fabrication, it is unrealistic to assume that the original design parameters of an SPR can be directly applied for real measurement.

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Before the calibration procedures aiming for the system parameters of an SPR's core, a preceding procedure is necessary for calibrating the power detectors (or amplitude detectors) embedded in an SPR. Such a step, often called the detector characterization (or linearization) in the literature [15-18], is responsible for transforming the output DC voltages of the detectors into the incident power levels observed by them. Since the SPR theorem operates on the basis of power levels, the step of detector characterization is unavoidable. In addition, it is of great significance, because any errors generated at this stage are likely to propagate to the last and ultimately manifest themselves as errors in the measured reflection coefficients. Therefore, optimizing the detector characterization by selecting the most suitable model is essential for the accurate measurement of an SPR.

For an SPR that is easy to implement in ICs, it can help perform on-chip measurement of scattering parameters [19] and reduce the testing costs of microwave and millimeter wave chips. Such capability is of great importance in maximizing the profit of commercial high-frequency on-chip components, such as the on-chip antennas [20, 21].

2. SPR Architecture and Design Parameters

As presented previously, the work in [3] enjoys excellent measurement performance and compact circuit architecture, which is especially favorable to ICs. Due to the limitation on the available chip area, this research specifically experiments on building an SPR by following the idea in [3] after a comprehensive evaluation. To explore the feasibility of performing on-chip reflection coefficient measurement at higher frequencies, the targeted operational frequency for the proposed SPR is set to be around 20 GHz. To work at such a high frequency, the proposed SPR is designed and fabricated in a more advanced semiconductor fabrication technology, i.e., the 0.13- μm IBM BiCMOS-8HP. Enclosed by the dotted rectangle, the architecture of the SPR is illustrated in Fig. 1. The signal generator is an external instrument, and the DUT denotes the various loads realized by an external programmable tuner. High-frequency sinusoidal signals are to be injected into Port 1 of the SPR chip and be divided into two ideally equivalent branches. One branch of signals will reach the DET3, whereas the other will flow through the phase shifter, hit the DUT via Port 2 of the SPR, and get reflected backward.

The four amplitude detectors, DET3, DET4, DET5, and DET6, are placed in specific places within the SPR to measure the power levels at the desired locations. The power levels sensed by the DET4, DET5, and DET6 should vary as the DUT changes, whereas the DET3 should ideally observe incident power unrelated to the DUT. Because the embedded detectors need to be small, robust, versatile, and operational at such a high frequency as 20 GHz, this research adopts those proposed in [22].

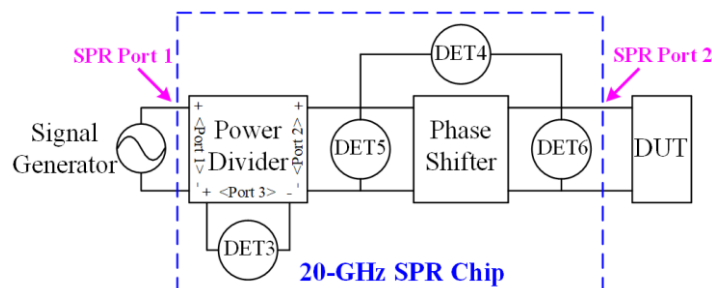


Fig. 1 The architecture of the SPR chip with two primary ports

With a core formed by a diode-connected NPN bipolar junction transistor, the schematics and design values of the amplitude detectors are shown in Figs. 2 and 3. The detector in Fig. 2 is for the DET4, DET5, and DET6, where the reflection coefficients looking into the detectors' input ports desire to be close to unity. As for the detector in Fig. 3, it is appropriate for the implementation of the DET3, which prefers a matched input impedance. The two input ports, Port 1 and Port 2, as specified in Figs. 2 and 3, signify that the simple diode-connected detector can work for differential detection. In addition, single-ended detection can be easily achieved by connecting the Port 2 of the detectors in Figs. 2 and 3 to the ground.

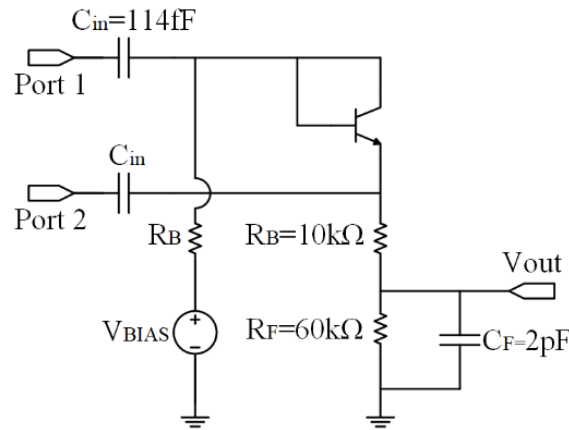


Fig. 2 The schematic and design values for the DET4, DET5, and DET6 in the SPR

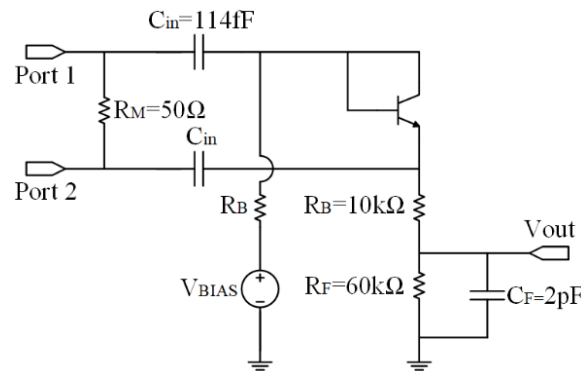


Fig. 3 The schematic and design values for the DET3 in the SPR

In addition to the four detectors as active devices, the SPR also contains two passive devices, the power divider and phase shifter. Contrary to the detectors, which actively detect incident power levels, the power divider and phase shifter create appropriate signal flows for the detectors to sense. Based on their different functions, the passive devices can be conveniently referred to as the core of the SPR, whereas the active devices are the peripheral.

The power divider in Fig. 1 is a three-port network that can split the input signal from Port 1 into two equivalent duplicates at Port 2 and Port 3. The schematic and design values are illustrated in Fig. 4, where the R_a , R_b , and Z_0 , are three resistors. As recommended by [3], the three resistors should have 50-Ω resistance. To maintain the accuracy of such low on-chip resistance, the three resistors are implemented by the low-sheet-resistance N+-diffusion layer in the 0.13-μm IBM BiCMOS-8HP technology. This research chooses to use the resistive type of power divider due to the smaller area yielded in the layout. On the other hand, a lossless power divider may occupy too large an area at 20 GHz. Despite a higher loss coming as a side effect, it is reasonably acceptable at 20 GHz.

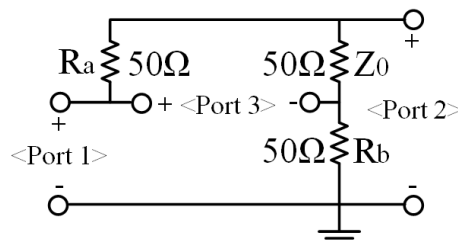


Fig. 4 The schematic and design values of the resistive power divider

The phase shifter in Fig. 1 is a two-port network that can cause a phase shift of approximately -60 degrees when signals travel from one port to the other. Similar to the reason for choosing the resistive power divider, the phase shifter in Fig. 1 is of lumped type, as in [3]. If a distributive phase shifter is adopted, the required layout area at 20 GHz may still be too large for on-chip implementation. Fig. 5 shows the schematic and design values of the phase shifter. The inductor, L , is implemented by a spiral inductor, and the capacitor, C , is realized by an MIM capacitor. Fortunately, the design values of the inductor and

capacitor both lie well within the region supported by the IBM BiCMOS-8HP technology. Furthermore, when designing the power divider and the phase shifter, it is feasible to keep the impedance looking into each port close to $50\ \Omega$. Such an effort can reduce the wave fluctuations due to mismatch and thus increase the accuracy of the SPR.

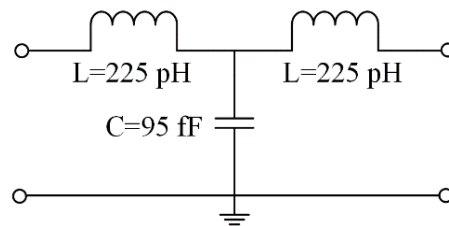


Fig. 5 The schematic and design values of the lumped phase shifter

3. Experimental Results and Discussion

The die micrograph of the fabricated SPR chip is shown in Fig. 6 with a chip size of 1.25 mm in width and 1 mm in height. The SPR circuit is enclosed by the dotted area, whereas the other circuits outside the area include a stand-alone detector and pads, which are independent of the SPR. It is observable that the chip size is heavily dominated by the pad ring with the SPR's area much less than $1.2\ \text{mm}^2$. In addition, expansive free space can be noticed in the SPR. This means the layout area of the SPR can be further reduced when the SPR is embedded in commercial chips for real use.

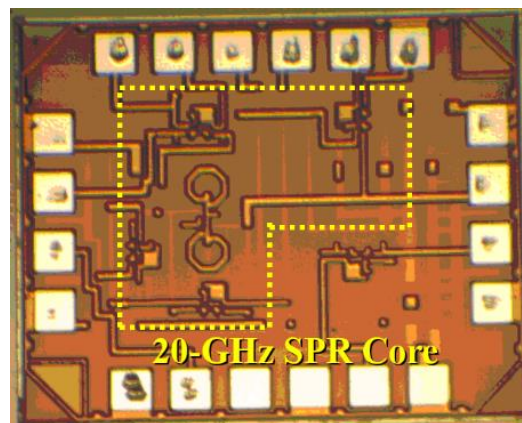


Fig. 6 The die micrograph of the 20-GHz SPR

The test set-up for the SPR is illustrated in Fig. 7, where the signal generator is the same as that in Fig. 1, and the programmable tuner corresponds to the DUT in Fig. 1. The signal generator can transmit 20-GHz sinusoidal signals at different amplitudes to the SPR as the input stimuli, whereas the programmable tuner can create different loads, which can be used for the SPR calibration and measurement. From Fig. 7, it can be known that a probe station with at least three arms is required. The signal generator and programmable tuner are connected to the SPR via two RF probes mounted on two opposite arms of the probe station. As for the third arm, it fixes a DC probe with multiple channels, where one is connected to a power supply to bias the amplitude detectors and four to four voltmeters to measure the detectors' output. Taken during the experiment, the lateral and vertical views of the probe station set-up are shown in Fig. 8, where the signal generator, power supply, and voltmeters are outside the scene.

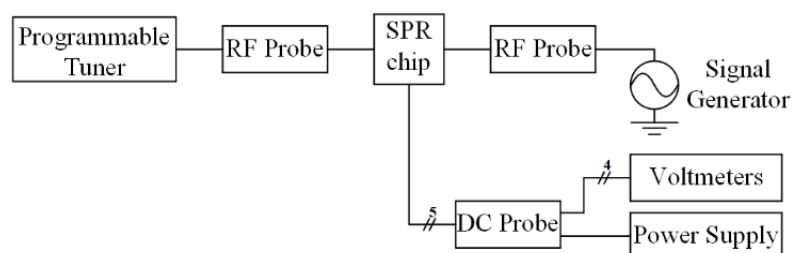


Fig. 7 The test set-up for the SPR chip

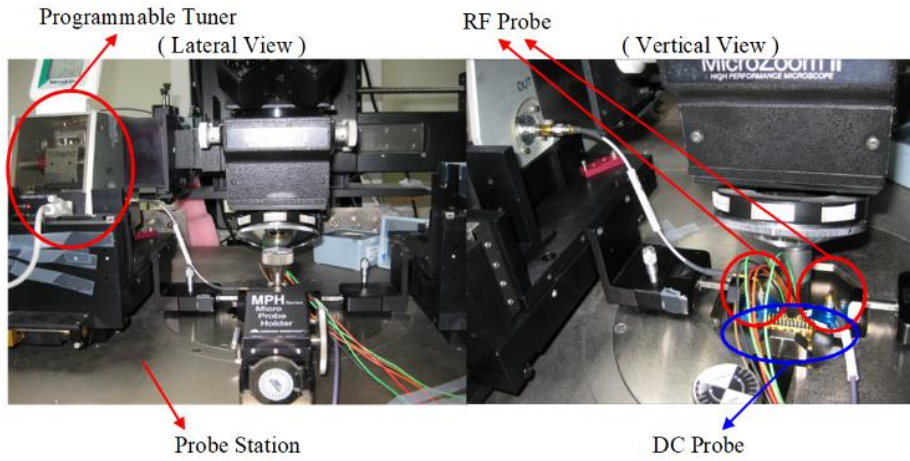


Fig. 8 The lateral and vertical views of the probe station set-up

To evaluate the performance of the fabricated SPR chip, it is necessary to perform various calibration procedures before the SPR can be used to measure different DUTs. The calibration procedures can be categorized into four parts, which are depicted in Fig. 9.

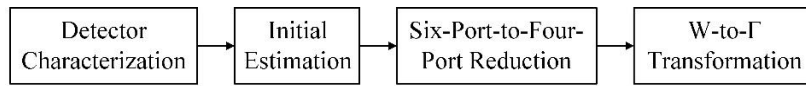


Fig. 9 The calibration procedures for the SPR chip

The first part of calibration is the detector characterization, which enables the transformation from the detectors' output voltages to the incident power levels at their input ports. Among the several models proposed in the literature [15-17], this research discovers that the model in [17] is the most compatible with the detectors being used. Hence, the model in [17] is used to perform the detector characterization with the following execution procedures.

First, the programmable tuner (Focus Microwaves: Model 67260) is used to generate five sliding terminations, which are five loads with reflection coefficients that have approximately equal magnitude but different phases. Although these sliding terminations are not necessarily required by the characterization procedure, they provide great convenience for further calibration steps. For each load, the signal generator (Agilent E8257D) is set to produce sinusoidal signals at 20 GHz with varying amplitudes. The amplitude sweeping is chosen to start from 0 volt to 1.04 volt with an 80-mV interval. During the process, the output of each embedded amplitude detector for each load is recorded, and the final result is shown in Fig. 10.

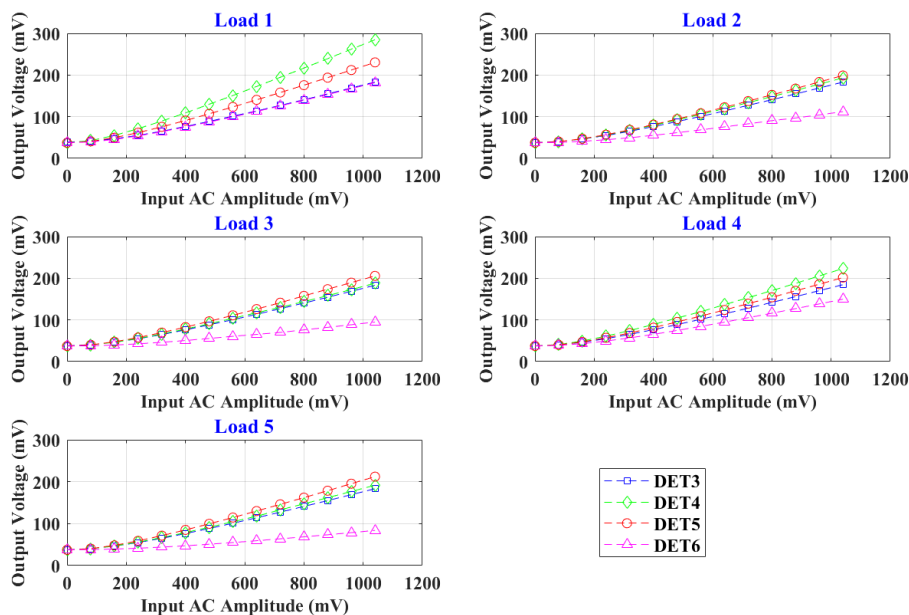


Fig. 10 The output voltages of the amplitude detectors with respect to different sliding terminations and input amplitudes

Unlike the other detectors, it is observable that the output voltages of the DET3 have no obvious change when the loads vary, a preferred attribute that is in the original design of the SPR. Then, by applying the measured data to Bergeault's method [17], the model parameters can be derived through the operation of multiple regression. The optimal model order is found to be five in this research. The systematic selection of the optimal model and model order will be presented in another individual paper in the future.

After all the detectors are properly characterized, it is feasible to infer the incident power of a detector from its output voltage. Hence, there is no need to adjust the signal generator to produce signals with different amplitudes. To avoid undesired noise interference and distortions caused by extreme voltages, the signal generator is, hereafter, set to output sinusoidal signals at 20 GHz with an intermediate amplitude of 640 mV.

The second calibration step is the "initial estimation," which aims to facilitate the following six-port-to-four-port reduction. As introduced in Section 1, the algorithm in [12] requires the least number of loads and reinforces the prevention of ill-conditioned estimations. Hence, this research adopts the suggestions from [12] and attempts to perform the initial estimation with the five loads that were used for the detector characterization. With both the measured data and detector models available, the initial estimation can be accomplished by using the data in Fig. 10 when the input AC magnitude equals 640 mV. Taking [12] into account, this research uses additional linear combinations of power ratios to enlarge the candidate pool to attain better estimation. For example, to derive the extremes of P_1 , besides the original pairs $\{P_1, P_2\}$ and $\{P_1, P_3\}$, this research employs six extra pairs, $\{P_1, P_2+P_3\}$, $\{P_1, P_2-P_3\}$, $\{P_1, P_2+2P_3\}$, $\{P_1, P_2-2P_3\}$, $\{P_1, 2P_2+P_3\}$, and $\{P_1, 2P_2-P_3\}$.

In searching for the extremes of the P_1 , P_2 , and P_3 , this research discovers two important findings. First, although [12] recommended that the median value among a group of extremes be retained, this research suggests that every extreme be examined before being considered a candidate. In other words, any extreme that does not result from an ellipse should be precluded. This can be done by inspecting the derived parameters of what is thought to be the coefficients of an ellipse either numerically or graphically. Fig. 11 illustrates a correct example by using the combination of $\{P_1, P_2\}$, whereas Fig. 12 shows a counterexample by using $\{P_1, P_2+2P_3\}$. The red squares are the power ratios corresponding to the five sliding terminations, whereas the curves in green and blue stars represent the shape of the equation organized by the extracted parameters. Although in both cases the curves fit the red squares well, the maximum and minimum derived by the extracted hyperbola equation in the second case should be abandoned. Second, this research discovers that if only a few combinations of power ratios can successfully derive elliptic coefficients, it is better to choose the optimal by scrutinizing the candidates graphically with equal axes. Fig. 13 demonstrates two comparative examples, where the two combinations, $\{P_3, P_2\}$ and $\{P_3, P_1-2P_2\}$, both derive coefficients of the ellipse. Focusing on the x-axis, the difference between the maximum and minimum of P_3 for the two cases is about equal. Hence, evaluating their suitability only through numbers may be inadequate and hardly able to decide. However, through visual observations, it becomes obvious that the extremes derived by the equation parameters extracted from the combination of $\{P_3, P_2\}$ are preferable because the shape of $\{P_3, P_2\}$ is less flat.

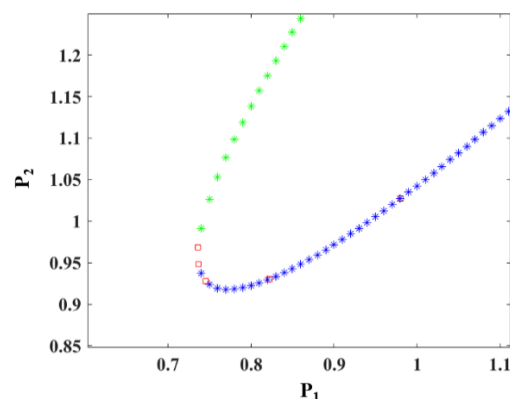


Fig. 11 The measured $\{P_1, P_2\}$ versus the shape of the equation organized by the extracted parameters

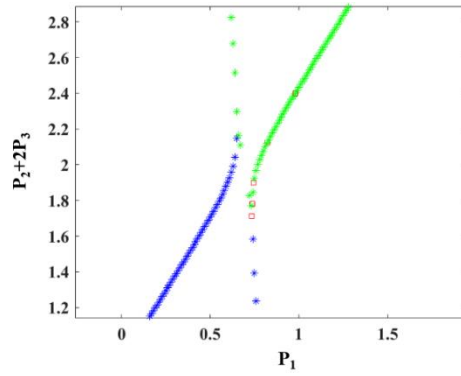


Fig. 12 The measured $\{P_1, P_2+2P_3\}$ versus the shape of the equation organized by the extracted parameters

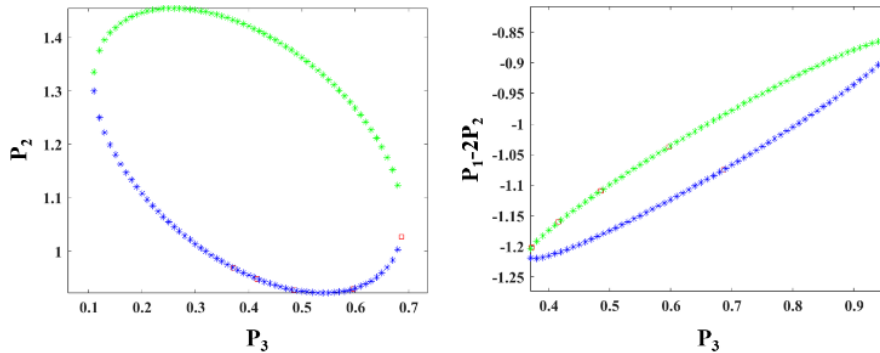


Fig. 13 The shape of the extracted equation extracted by $\{P_3, P_2\}$ is less flat than that extracted by $\{P_3, P_1-2P_2\}$

After the extremes of P_1 , P_2 , and P_3 are derived, the five parameters of interest, Z , R , A , B , and C , become available. Subsequently, the next step goes to the “six-port-to-four-port reduction,” which is used to examine whether the estimated system parameters can be further refined. Several methods are available in the literature [7, 23-24] and this research utilizes the constraint formula proposed by [7]. When this step is finished, all the system parameters of the SPR are finalized. This means the reflection coefficient of a DUT can be measured based on the voltages reported by the four amplitude detectors. However, such a derived result is on the W -plane, whereas the real reflection coefficient lies on the Γ -plane. Hence, it is necessary to perform the fourth step, the “ W -to- Γ -Transformation,” which can be simply achieved by using three known loads to acquire the three unknowns in the bilinear equation. To exploit the five sliding terminations, this research applies all of them to this final step of calibration.

After the completion of the four calibration procedures in Fig. 9, the SPR chip is fully calibrated and ready to measure various DUTs. To demonstrate the performance of the SPR chip, this research uses the programmable tuner to create six additional loads. With the initial five loads applied for calibration, there are totally eleven loads available for testing. Fig. 14 shows the output voltages of the four detectors with respect to the six additional loads, with load numbers from six to eleven. As for the sliding terminations, numbered from one to five, the corresponding detector outputs can be known by consulting the output voltages corresponding to the input AC amplitude at 640 mV in Fig. 10.

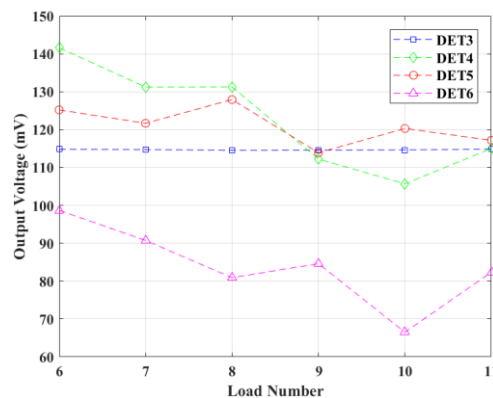


Fig. 14 The output voltages of the amplitude detectors corresponding to load 6 to load 11

By applying the measured voltages to the system parameters derived through the calibration procedures, the reflection coefficients measured by the SPR chip can be obtained. To verify the correctness of the SPR measurement, an Agilent E8361A vector network analyzer (VNA) is used to measure the same eleven loads. The measured reflection coefficients are summarized in Table 1, where the “Tuner Position” column includes the position commands given to the tuner in order to create the loads. The “Reflection Coefficient (VNA)” column shows the reflection coefficients measured by the commercial VNA, whereas the “Reflection Coefficient (SPR)” column shows the reflection coefficients measured by the SPR chip. The two columns of data observably match each other very well, proving the great performance of the SPR.

Table 1 Specifications of loads and measurement results

Load Number	Tuner Position		Reflection Coefficient (VNA)		Reflection Coefficient (SPR)	
	Pos1	Pos2	Magnitude	Phase (deg)	Magnitude	Phase (deg)
1	835	2685	0.51261	-4.1517	0.51282	-4.5807
2	35	2440	0.50261	86.339	0.49840	84.0508
3	2000	2550	0.49638	112.89	0.49881	112.2072
4	685	2505	0.50046	46.359	0.50203	48.2765
5	1800	2620	0.50004	130.64	0.50083	132.1678
6	735	2545	0.50814	39.250	0.49939	41.8899
7	585	2465	0.50423	55.094	0.54478	58.8780
8	280	2054	0.35310	73.247	0.37031	69.0118
9	35	2685	0.73969	71.850	0.74150	69.2505
10	2000	2685	0.70062	100.52	0.66060	100.6245
11	180	2600	0.64998	73.700	0.66181	72.3899

The measured reflection coefficients of the five sliding terminations are graphically shown in Fig. 15, where the circles and stars represent the data measured by the VNA and SPR, respectively. It is noteworthy that tuning the programmable tuner to achieve a desired reflection coefficient is not a task sure to succeed at such a high frequency as 20 GHz. This is due to the limitation of the programmable tuner itself. In other words, the tuning process can only proceed in a trial-and-error manner without a table of position commands that can be specifically referred to. In addition, it was found during the experiment that reflection coefficients at certain areas on the Smith chart seem unlikely to be created by the tuner. This difficulty explains why the five sliding terminations, theoretically preferring an even distribution on a circle, occupy only a portion of the circle instead.

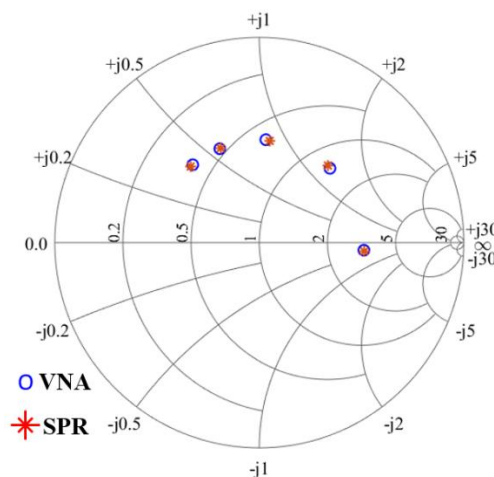


Fig. 15 The measured reflection coefficients of the five sliding terminations by the VNA and SPR at 20 GHz

Fig. 16 depicts the measured reflection coefficients of all the eleven loads, as listed in Table 1. It is noteworthy that the reflection coefficients measured by the VNA, denoted by the blue circles, are in great proximity to those measured by the SPR, denoted by the red stars. Using the reflection coefficients measured by the VNA as the standard, the maximum discrepancy in absolute value between the reflection coefficients measured by the VNA and those by the SPR chip can be found to be about 0.05, i.e., -26 dB. Compared to the maximum error of 0.04 at 3 GHz in [3], a measurement error of 0.05 at 20 GHz is reasonable and satisfactory.

With the primary ports, Port 1 and Port 2, defined in Fig. 1, Fig. 17 shows the S_{21} of the SPR chip measured by the VNA. As can be seen, the magnitude of S_{21} at 20 GHz is about 0.27, which is less than the original design value, 0.5, due to the extra loss along the transmission path. Such loss reduces the incident power levels at the input ports of the detectors. Moreover, from Fig. 1, it can be easily identified that the DET6 should suffer the most severe signal loss among the four detectors. Such an inference can be reconfirmed in Fig. 10 and Fig. 14. As the operational frequency continues to rise, it can be expected that the intensity of signal loss will get more aggravated. Ultimately, the detectors will end up having no signals to detect, causing the failure of the SPR chip. Given this foreseeable problem, for an SPR aiming to work at higher frequencies, it is recommended that its core be rethought and redesigned.

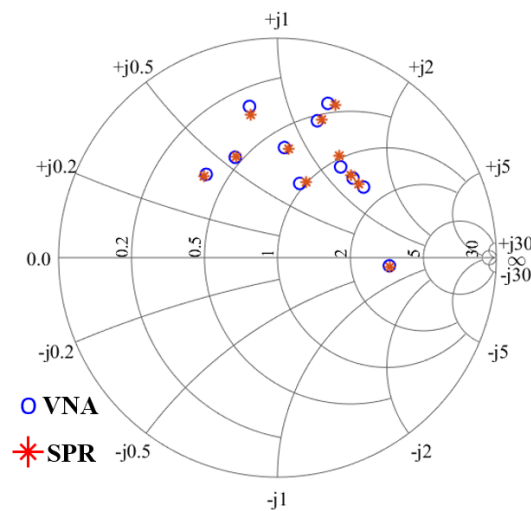


Fig. 16 The measured reflection coefficients of the eleven loads by the VNA and SPR at 20 GHz

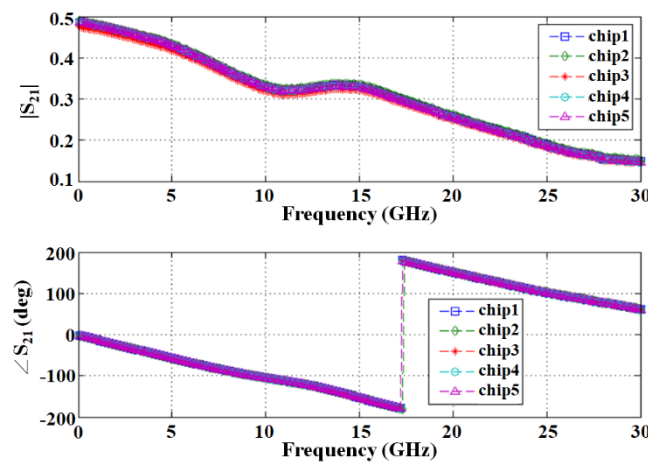


Fig. 17 The measured S_{21} of the SPR chip

Despite the extra loss along the transmission path and the difficulty in preparing well-distributed sliding terminations for calibration, the SPR chip still demonstrates excellent accuracy in measuring the reflection coefficients of the DUTs. The reason is mainly due to the solid design and calibration theorems behind the SPR as well as the advanced semiconductor technologies available in modern times. In sum, the SPR has proved to be a reliable circuit that is applicable to the on-chip measurement of the reflection coefficient.

For the imperfection in the additional signal loss among the transmission path, it can be solved by reducing the redundant wire length in the SPR, as in Fig. 6. Since the layout in Fig. 6 is drawn under a given chip size, it aims to accommodate the maximum use of the silicon area and to cooperate with the port and pad placement. In the future, when the SPR is embedded in a commercial chip for real use, the extra transmission path will be naturally and easily reduced. For the imperfection in finding some well-distributed sliding terminations, this research aims to resort to building some embedded adjustable calibration standards in the future.

4. Conclusion

This paper proposes an on-chip SPR chip capable of measuring the reflection coefficients of DUTs at around 20 GHz. By exploiting various recommendations from different previous works in the literature and by carefully examining the calibration results, the SPR chip demonstrates excellent measuring ability in the face of imperfect calibration devices and excessive signal loss. Among the eleven loads used for testing, the maximum error is approximately -26 dB, which is satisfactory compared to the previous work with an error of -28 dB at 3 GHz. The size of the SPR chip is 1.25 mm in width and 1 mm in height, which possesses expansive free space that can be further removed in the future when necessary.

Conflicts of Interest

The author declares no conflict of interest.

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