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A New Efficient Topology of Single-Phase Five-level Inverter for PV System

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Abstract

This paper presents the design, simulation, and implementation of a new single-phase five-level inverter, for photovoltaic systems, with a reduced number of power switches and fewer gate-drivers power supply. This multilevel inverter consists of a high step-up DC-DC converter, a switched-capacitor converter, and a full bridge converter. The proposed topology is used to deliver optimal AC voltage and current with fewer harmonics to the loads by controlling the high step-up DC-DC converter with a small duty cycle. A prototype of a 200W rated power feeding an inductive load from solar panels is tested by simulation and experiment. A maximum power point tracking method and a pulse width modulation technique are presented and evaluated under normalized criteria for voltage, frequency, and total harmonics distortion (THD). The experimental results show that the proposed multi-level inverter is an efficient converter to supply power energy from solar panels to industrial machines such as single phase induction motors.

Keywords: photovoltaic system, switched capacitor converter, multilevel inverter, boost converter

1. Introduction

Wind and solar energy are currently being used to reduce the consumption of fossil fuels and decrease greenhouse gas emissions. Power electronics techniques and converters play a crucial role in this energy transition. Researchers and industrialists continue to improve these fields by developing new solutions that minimize both component count and manufacturing costs [1].

In photovoltaic (PV) systems, in which electricity is generated by converting the energy produced by solar panels from DC to AC, the use of high-efficiency inverters is necessary. Classical inverters pose certain problems such as high switching losses, bulky output filters, and considerable harmonics.

Multilevel inverters can overcome these problems. They provide sinusoidal AC waveforms with fewer harmonics and output filters that are of reduced size and sometimes eliminated. They can be used in high-power applications with low switching losses across the power switches, thus increasing the efficiency of the PV chain conversion [2]. Standard multilevel inverters are classified into three categories: cascade H-bridge inverter, flying capacitor inverter, and neutral point clamped inverter [3]. From these categories, several topologies of multilevel inverters are derived by utilizing symmetric, asymmetric, and hybrid arrangements [4]. The switched capacitor converter (SCC) is one of the derived topologies. It is used as a step-up converter, delivers multilevel DC voltage, and can be tied with classical inverters to obtain multilevel AC waveforms. Many SCC circuits have been discussed in the literature [5-7]; however, they are used for systems operating at high frequency and cannot supply power energy for systems operating at low frequencies such as 50 Hz and 60 Hz.

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This paper presents the design, simulation, and experimental testing of a new single-phase five-level inverter for photovoltaic system applications. This photovoltaic inverter is novel because it combines the new high step-up DC–DC converter (HSUC), proposed in [8], with the SCC [9-11] and conventional full bridge converter (FBC). By utilizing the proposed combination, the HSUC is controlled with a small duty cycle thus reducing the switching losses across its power switches. The output AC voltage is sinusoidal in shape with five levels, and the total number of power switches and gate driver power supply are reduced compared to conventional multilevel inverters. This multilevel inverter presents many advantages over a classical inverter composed of a conventional boost converter and a full bridge converter used in a PV chain conversion, where the duty cycle is very high and the output AC voltage has two or three levels [12].

The proposed topology is tested using the maximum power point tracking method (MPPT) to verify the ability of the system to extract maximum power energy from solar panels. In addition, an efficient pulse width modulation (PWM) control method is applied, that enables the system to deliver good output AC waveforms with fewer harmonics without using output filters. An experimental prototype of a 200 W rated power is fabricated at the laboratory and tested by supplying power energy from solar panels to a single-phase induction motor, in order to validate the simulation results and to confirm the high efficiency of the proposed multilevel inverter.

This paper is organized as follows: Section 2 describes the proposed single-phase five-level inverter, Section 3 presents the control strategies used, Section 4 presents the simulation results, Section 5 presents the experimental results, and Section 6 presents the conclusion.

2. Description of the proposed Single Phase Five-Level Inverter

The topology of the proposed single phase five-level inverter is shown in Fig. 1.It consists of a single input DC voltage (Vin) from solar panels (PV), the HSUC, and the DC-AC five-level converter (FLC).

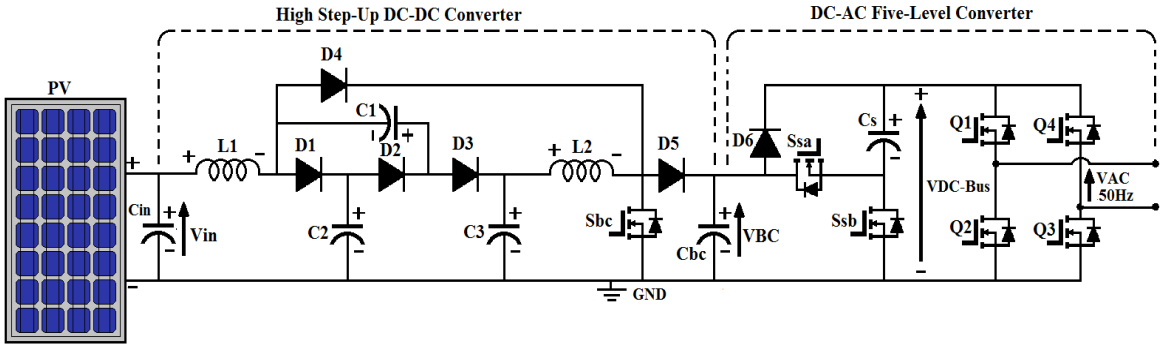


Fig. 1 Topology of the proposed photovoltaic multilevel inverter

2.1. Solar panels

Solar panels are made of an electrical assemblage of small solar cells which produce DC current through the photovoltaic effect by absorbing photons from sunlight. A simple model of a solar cell is shown in Fig. 2; it's based on a current source, single diode, parallel resistance and a series resistance.

The expression of the generated current from this model is shown in Eq. (1) [1, 11-13]:

$$I = Iph - Is(exp\frac{q(V + RsI)}{NKT} - 1) - \frac{(V + RsI)}{Rp} \quad (1)$$

where I is the output current, Is is the reverse saturation current of the diode, Iph is the photocurrent, N is the ideality factor of the diode, V is the output voltage, q is the electron charge (1.60217662×10^{-19}coulombs), K is the Boltzmann constant ($1.38064852 \times 10^{-23}$ m^2 kg s^{-2} K^{-1}), and T is the junction temperature.

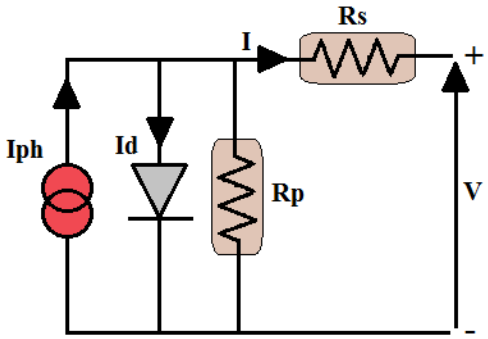


Fig. 2 Simple model of a solar cell

2.2. High Step-Up DC-DC converter

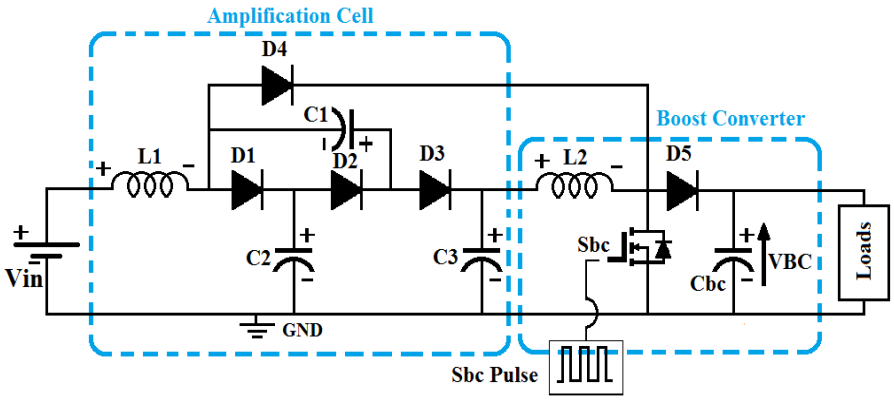


Fig. 3 The used high step-up DC-DC converter

The used HSUC is shown in Fig. 3. It's composed of an amplification cell tied with a simple boost converter. The amplification cell consists of one inductor (L1), four diodes (D1, D2, D3, and D4), and three capacitors (C1, C2 and C3), while the boost converter consists of one inductor (L2), one diode (D5), one power switch (Sbc), and one capacitor (Cbc).

This DC-DC converter is used to deliver high output voltage (*VBC*) from a lower voltage (*Vin*). *VBC* and *Vin* are related to one equation expressed in Eq. (2) [8]:

$$\frac{VBC}{Vin} = \frac{2}{(1-D)^2} \tag{2}$$

where D is the duty cycle of the control signal of this DC-DC converter($0 \leq D \leq 1$).

The operation of the HSUC and the sizing of the important used elements are presented in detail as follows, which is not the case of [8]: By considering that Sbc is controlled with a pulse signal having a duty cycle (D), and a chosen frequency (Fs); two important modes are discussed.

(1) Mode I: When Sbc is ON, the diodes D4 and D2 are forward biased; the remaining diodes (D1, D3, and D5) are reversely biased, as shown in Fig. 4 (a).

In this mode; the inductor L1 is charged by current from Vin through D4 and Sbc; the capacitors C1 and C2 are charged and discharged in order to get balanced state through D2, D4, and Sbc; the inductor L2 is charged by current from VC3 through Sbc; the capacitor Cbc supply power energy to the load.

The derived equations from mode (I) are presented as follow:

$$VL1 = Vin \tag{3}$$

$$VC1 = VC2 \tag{4}$$

$$VL2 = VC3 \tag{5}$$

(2) Mode II: When Sbc is OFF, the diodes D1, D3, and D5 are forward biased; the remaining diodes (D2 and D4) are reversely biased, as shown in Fig. 4 (b).

In this mode; the capacitor C2 is charged by voltage from *Vin* and *VL*1 through D1; the capacitor C3 is charged by *VC*1 through D3; the inductor *L*2 supply power energy to the load and the capacitor Cbc.

The derived equations from mode (II) are presented as follow:

$$VL1 = Vin - VC2 \tag{6}$$

$$VC3 = VC1 + VC2 \tag{7}$$

The inductor L1 is charged and discharged with current during the period Ts; for this:

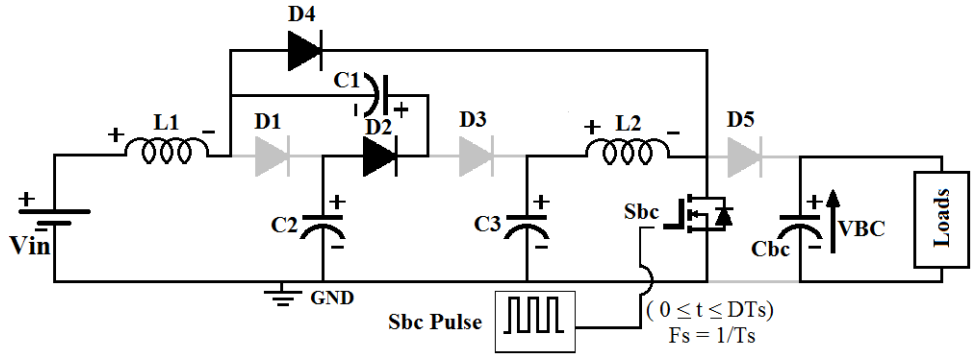
$$VL1 \times D + VL1 \times (1 - D) = 0 \tag{8}$$

From Eq. (3), Eq. (6), and Eq. (8):

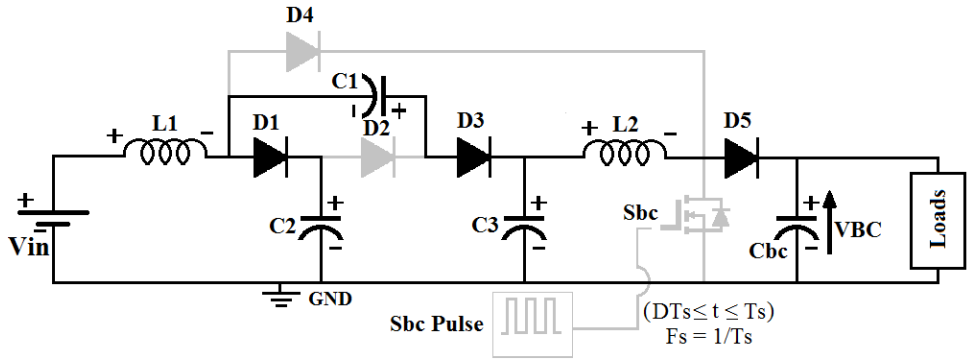
$$Vin \times D + (Vin - VC2) \times (1 - D) = 0 \tag{9}$$

From Eq. (4), Eq. (7), and Eq. (9):

$$VC3 = \frac{2Vin}{(1 - D)} \tag{10}$$



(a) Sbc-ON state



(b) Sbc-OFF state

Fig. 4 The operating states of the power switch Sbc

As indicated previously, the used HSUC contains an amplification cell tied with a conventional boost converter; for this, by considering the related equation between the input voltage and the output voltage of a boost converter [14]:

$$VBC = \frac{VC3}{(1-D)} \tag{11}$$

From Eqs. (10)-(11), the related equation between *VBC* and *Vin* is demonstrated in Eq. (12):

$$\frac{VBC}{Vin} = \frac{2}{(1-D)^2} \tag{12}$$

Fig. 5 shows the obtained waveforms during mode I and mode II.

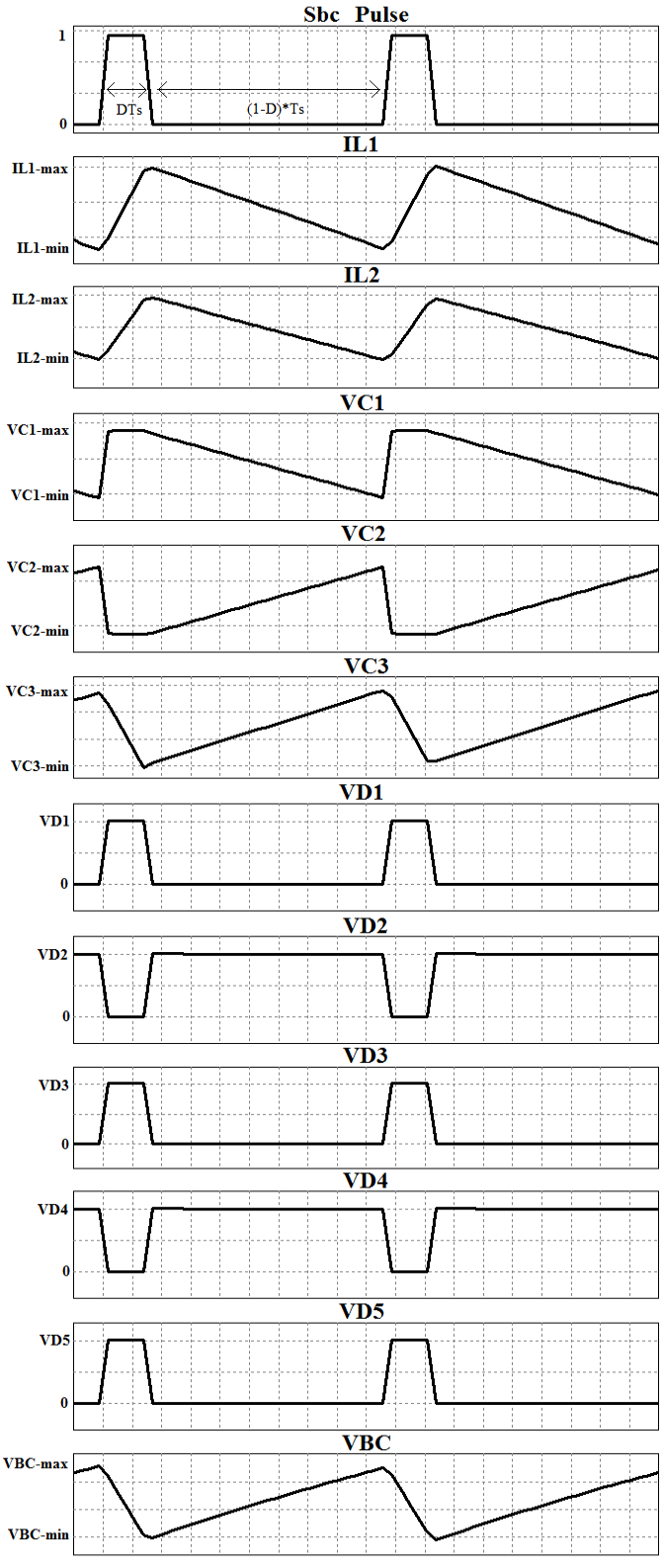


Fig. 5 Waveforms of the used DC-DC converter during continuous modes (Mode I and Mode II)

In order to use the DC-DC converter in the correct form, the values of the different used elements have to be calculated. For a conventional boost converter, the values of its input inductor (Lin) and its output capacitor (Cout) can be determined using Eq. (13) and Eq. (14) [14].

$$Lin = \frac{Ve \times D}{\Delta IL \times Fs} \tag{13}$$

$$Cout = \frac{Is \times D}{\Delta VC \times Fs} \tag{14}$$

where D and Fs are respectively the duty cycle and the frequency of the control signal; Ve and Is are respectively the input voltage and output current; ΔIL and ΔVC are respectively the ripples of the input current and the output voltage.

By similarity from Eq. (13) and Eq. (14), the values of the inductor L2 and the capacitor Cbc can be determined using Eq. (15) and Eq. (16).

$$L2 = \frac{VC3 \times D}{\Delta IL2 \times Fs} \tag{15}$$

$$Cbc = \frac{Is \times D}{\Delta VBC \times Fs} \tag{16}$$

The studied HSUC is used to step-up voltage (Step-down current); for this, by similarity from Eq. (10), the current across the inductor L2 can be determined using Eq. (17).

$$IL2 = \frac{(1-D) \times IL1}{2} \tag{17}$$

From Eq. (10), Eq. (15), and Eq. (17), the expression of L2 can be simplified.

$$L2 = \frac{4 \times D \times Vin}{(1-D)^2 \times \Delta IL1 \times Fs} \tag{18}$$

The inductor L1 is charged with current when Sbc is ON, and discharged when Sbc is OFF; for this, by similarity from Eq. (13), the inductor L1 can be determined using Eq. (19).

$$L1 = \frac{Vin \times D}{\Delta IL1 \times Fs} \tag{19}$$

The capacitor C3 is discharged when Sbc is ON, and charged when Sbc is OFF; for this, by similarity from Eq. (14), the capacitor C3 can be determined using Eq. (20).

$$C3 = \frac{IC3 \times D}{\Delta VC3 \times Fs} = \frac{IL2 \times D}{\Delta VC3 \times Fs} \tag{20}$$

From Eq. (17) and Eq. (20), the expression of C3 can be simplified.

$$C3 = \frac{IL1 \times D \times (1-D)}{2 \times \Delta VC3 \times Fs} \tag{21}$$

From Eq. (4), Eq. (7), and Eq. (21), the capacitors C1 and C2 can be determined using Eq. (22).

$$C1 = C2 = \frac{C3}{2} = \frac{IL1 \times D \times (1-D)}{4 \times \Delta VC3 \times Fs} \tag{22}$$

2.3. DC-AC five-level converter

The used DC-AC FLC is shown in Fig. 6. It's composed of a switched-capacitor converter (SCC), and a full bridge converter (FBC). The SCC consists of two power switches (Ssa and Ssb) and one capacitor (Cs), while the FBC consists of four power switches (Q1, Q2, Q3, and Q4).

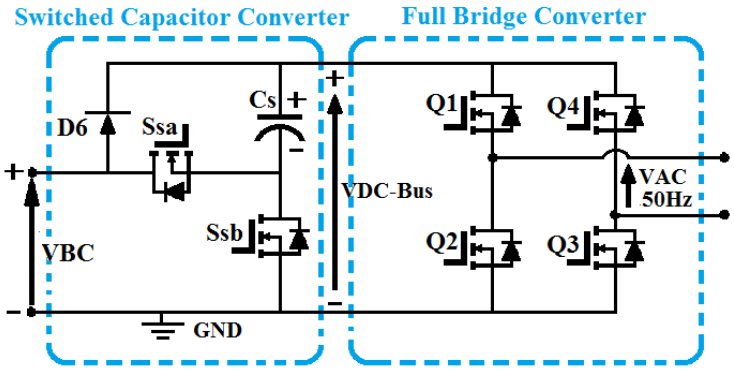
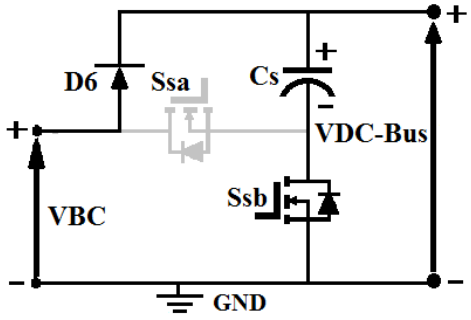
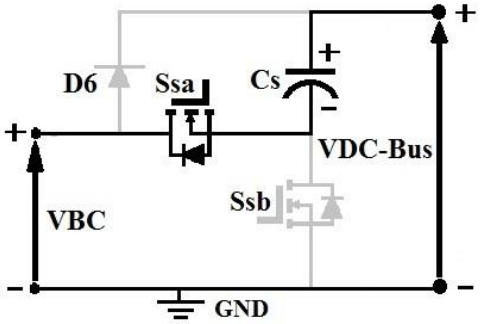


Fig. 6 The used DC-AC five-level converter

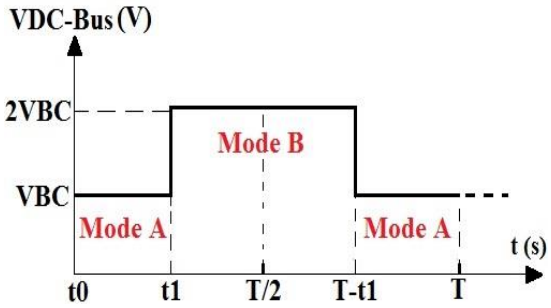
The SCC delivers an output DC voltage (VDC-Bus) greater than VBC by switching the capacitor Cs in series and in parallel. The operation of this converter is described as follows:



(a) Mode A of the SCC



(b) Mode B of the SCC



(c) DC-Bus voltage waveform

Fig. 7 The two operating modes of the SCC with the generated DC-Bus voltage waveform

(1) Mode A: When the switch Ssb is ON (Ssa is OFF); the diode D6 is forward biased. In this case, the capacitor Cs is charged by VBC, as shown in Fig. 7 (a). The expression of the DC-Bus voltage is developed in Eq. (23):

$$VDC - Bus = VCs = VBC \tag{23}$$

(2) Mode B: When Ssa is ON (Ssb is OFF); the diode D6 is reversely biased. In this case, the capacitor Cs is discharged, as shown in Fig. 7 (b). The expression of the DC-Bus voltage is developed in Eq. (24):

$$VDC-Bus = VCs + VBC = 2 \times VBC \tag{24}$$

From Eq. (23) and Eq. (24), the SCC generates a positive staircase waveform which begins from VBC and ends at 2VBC, repeated at each period (T), as shown in Fig. 7 (c), where [t0, t1] and [t1, T-t1] are the times' intervals for mode A, mode B respectively.

To calculate the value of the used capacitor *Cs*, it's necessary to know [15-16]:

(1) The value of the output AC current supplied to the AC load and the difference phase (φ) between this current and the output AC voltage.

(2) The length of time of each step of DC Bus staircase waveform.

By using the two conditions described above, the amount charge *QCs* of the capacitance *Cs* is firstly calculated using Eq. (25):

$$QCs = \int_{t1}^{T-t1} Iout \times sinus(2\pi ft - \varphi) \times dt \tag{25}$$

where f and Iout are respectively the frequency of the output AC voltage and the amplitude of the AC current supplied to the load, [t1; T-t1] is the time interval which is corresponded to longest discharging cycle (LDC) of *Cs*, as shown in Fig. 7 (c) and detailed in mode B.

By considering that Δ*VCs* is the chosen voltage ripple across the capacitor *Cs*, the value of its capacitance can be calculated using Eq. (26):

$$Cs \geq \frac{QCs}{\Delta VCs} \tag{26}$$

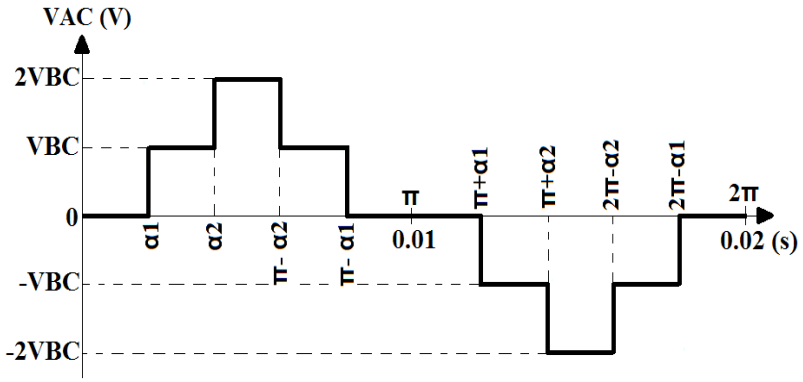


Fig. 8 Output AC voltage waveform

The FBC is used to convert VDC-Bus to an AC voltage (VAC) with a specified frequency (50Hz in this study). Table 1 summarizes the switching states of all used power switches in the DC-AC FLC, and Fig. 8 shows the obtained VAC voltage waveform.

Table 1 Switching states of the power switches

Switching states						**VAC**
Q1	**Q2**	**Q3**	**Q4**	**Ssb**	**Ssa**	
ON	OFF	ON	OFF	OFF	ON	**+2VBC**
ON	OFF	ON	OFF	ON	OFF	**+VBC**
OFF	ON	ON	OFF	OFF	OFF	**0**
ON	OFF	OFF	ON	OFF	OFF	**0**
OFF	ON	OFF	ON	ON	OFF	**-VBC**
OFF	ON	OFF	ON	OFF	ON	**-2VBC**

3. Control Strategies of The Studied Multilevel Inverter

3.1. Control method of the used HSUC with maximum power point tracking

The MPPT methods are used in photovoltaic systems to extract maximum power energy from solar panels under different climatic conditions. Several methods of MPPT are presented in the literature [17]. The algorithm Perturb and Observe (P&O) still the easy way to implement the MPPT; This method is based on measuring input voltage (Vin) and input current (Iin) from solar panels, and operates by perturbing Vin to extract maximum power energy, as shown in Fig. 9. Although some problems can appear with this method, such as oscillations around the maximum power point (MPP); the P&O was used to test the robustness of the studied DC-DC converter in critical conditions. Fig. 10 shows the implementation of the chosen MPPT method with the HSUC.

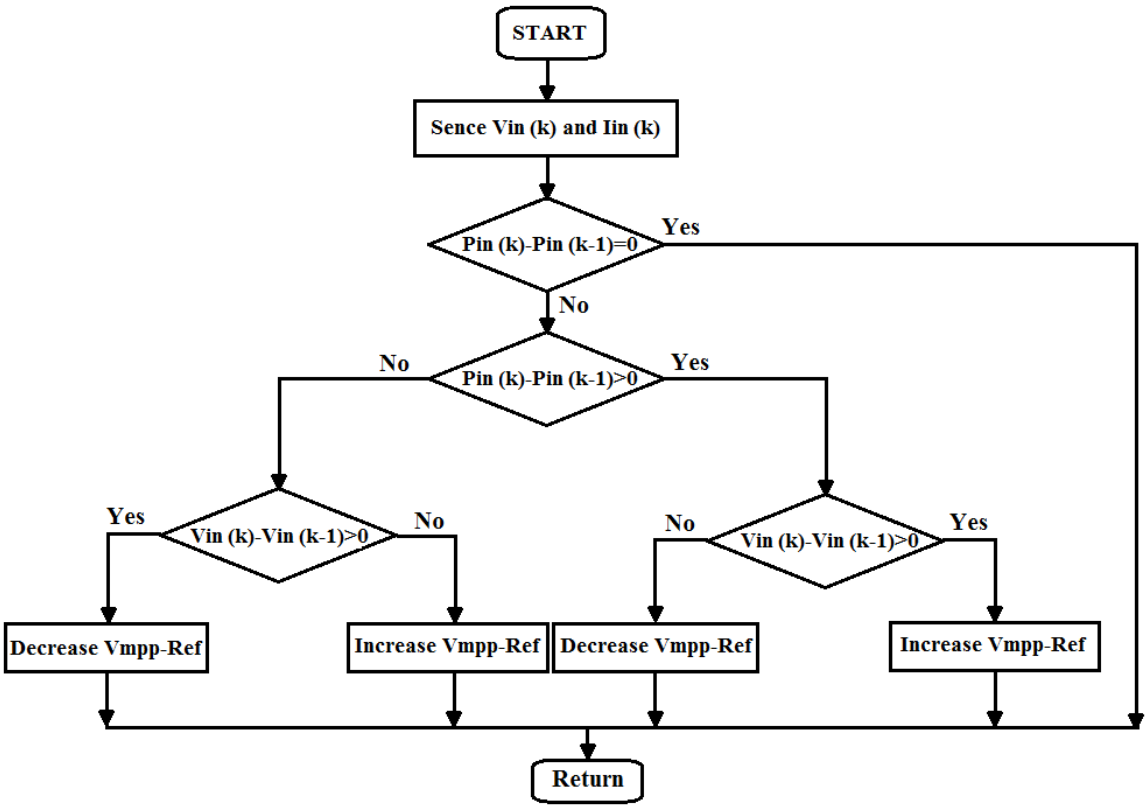


Fig. 9 Flowchart of the P&O method

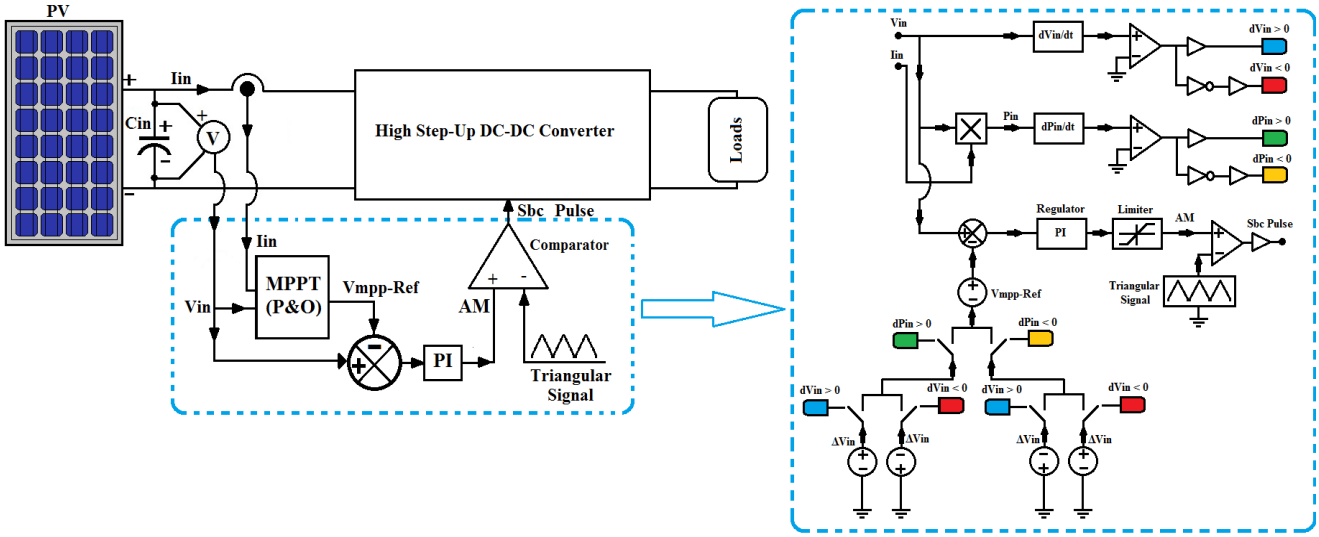


Fig. 10 P&O method with the studied DC-DC converter

The used MPPT is equipped with a PI regulator to minimize the difference error between the sensed voltage Vin and Vmpp-Ref, and also to faster the response of the MPPT method to any sudden variation in climatic conditions [14-18]. The generated signal (AM) from the PI regulator is compared with a high-frequency triangular signal to generate the control signal with the appropriate duty cycle for the HSUC.

3.2. Control method of the used DC-AC FLC with PWM method

In order to control the studied DC-AC FLC with high-frequency modulation technique, an efficient and simple pulse width modulation (PWM) method is applied [19-20]. It's based on comparing two identical high-frequency triangular carrier signals (Carr1 and Carr2) with a rectified low-frequency (50Hz) sinusoidal signal (Ref), as shown in Fig. 11.

The RMS value of the output AC voltage (VAC) is controlled with the proposed PWM method by varying the modulation index MI which is expressed in Eq. (27).

$$MI = \frac{AR}{2AC} \tag{27}$$

where *AR* and *AC* are respectively the amplitudes of the rectified signal (Ref) and the carrier signals.

In order to control the power switches used in the DC-AC FLC, and to respect the charge and discharge cycle of the capacitor Cs, as shown previously in Mode A and Mode B with the proposed PWM method, logic gates are used for comparing the carrier signals (Carr1 and Carr2) with the reference signal (Ref), as described in Table 2. Q3 and Q4 are controlled with two opposite square wave pulses (with a frequency of 50Hz). The generated waveforms of VDC-Bus and VAC with the PWM method are shown in Fig. 11.

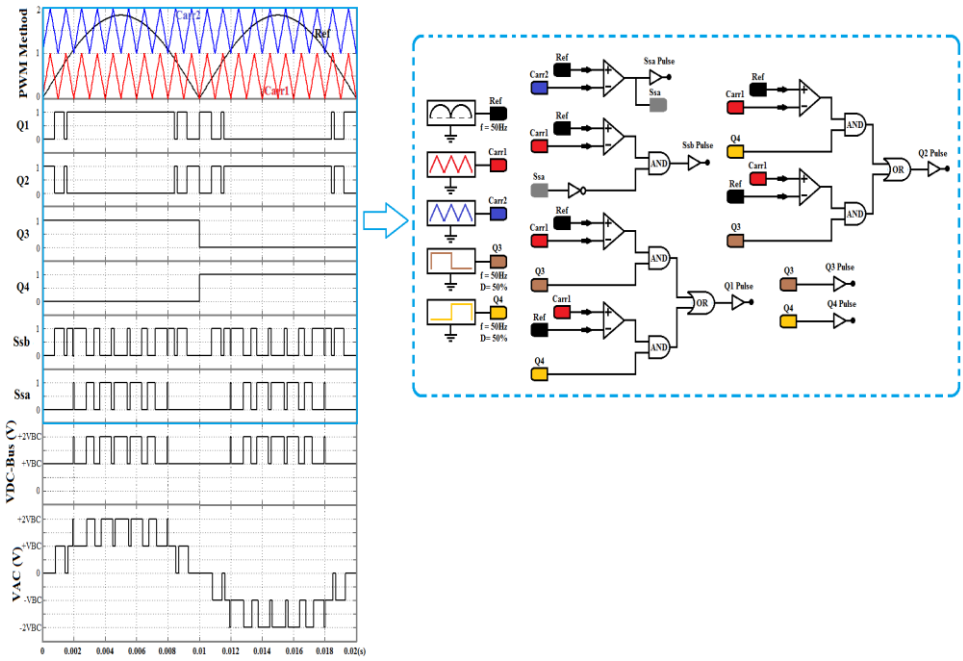


Fig. 11 The used PWM method with the obtained gate pulses and the generated waveforms

Table 2 Switching conditions of the power switches with logic gates

Conditions	ON switches
{(Ref >= Carr1) AND (Q3 pulse)} OR{(Ref <= Carr1) AND (Q4 pulse)}	Q1
{(Ref >= Carr1) AND (Q4 pulse)} OR{(Ref <= Carr1) AND (Q3 pulse)}	Q2
(Ref >= Carr2)	Ssa
{(Ref >= Carr1) AND (NOT Ssa pulse)}	Ssb

4. Simulation results

A prototype of a 200W rated power of the proposed photovoltaic multilevel inverter is designed with ideal components and tested on PSIM Software [21]. Two identical solar panels coupled in series are used as a DC source. Table 3 resumes the values of the main elements used in the proposed multilevel inverter, and Table 4 resumes the electrical parameters of the used solar panels.

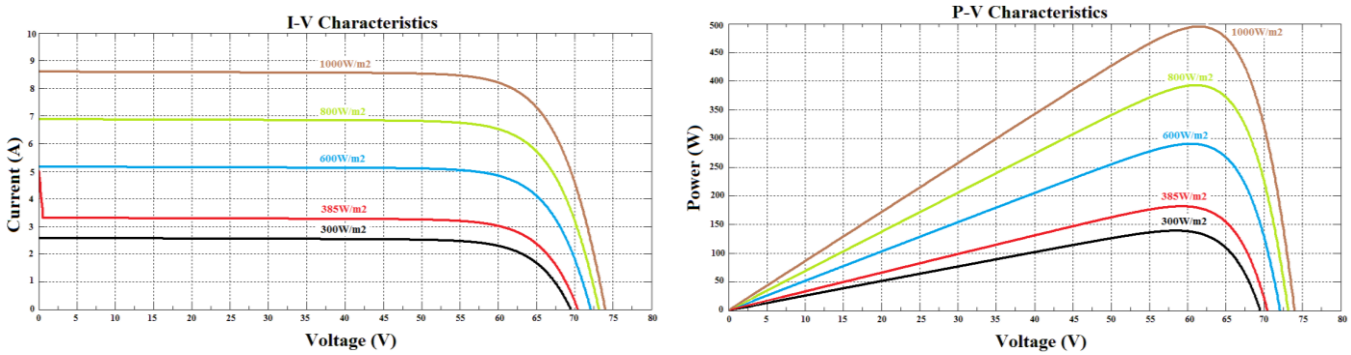
Table 3 Values of the used elements in the multilevel inverter

Elements	Values
Inductors L1 and L2	2mH; 12mH
Capacitors Cin, C1, C2, C3, Cbc, and Cs	240µF;120µF; 120µF; 240µF; 750µF; 750µF

Table 4 Parameters of one solar panel under 1000W/m2 and 25℃

Parameters	Values
Maximum power (Pmax)	240W
Voltage at Pmax (Vmp)	29.9V
Current at Pmax (Imp)	8.03A
Short-circuit current (Isc)	8.60A
Open-circuit voltage (Voc)	37.0V

Fig. 12 shows the obtained I-V characteristics (a) and P-V characteristics (b) of the model of the two solar panels coupled in series, with different irradiation levels, and constant temperature level (25℃).



(a) I-V characteristics (b) P-V characteristics

Fig. 12 I-V characteristics and P-V characteristics of the two solar panels coupled in series

4.1. Simulation results of the used HSUC with MPPT

The HSUC was tested with the proposed MPPT method shown in Fig. 10. In accordance with its rated power (200 W); the variable irradiation levels between 300 W/m2 and 385 W/m2 were selected. In this case, the maximum power energy available across the two solar panels varied between 140 and 180 W, as shown in Fig. 12 (b). The important used parameters in this simulation test are listed below:

(1) Vmpp-Ref of the MPPT is 59V.
(2) The frequency of the triangular signal (Fs) used in the comparison as shown in Fig. 10 is 31 kHz.
(3) The output load is constant with a rated power of 200W.
(4) From 0 to 0.5 second and 1 to 1.5 second, the solar irradiation level is 385W/m^2 and the temperature level is 25°c.
(5) From 0.5 to 1 second and 1.5 to 2 second, the solar irradiation level is 300W/m^2 and the temperature level is 25°c.

Fig. 13 shows the obtained voltage (Vin) and current (Iin) from the two solar panels under this test. From the obtained results, the voltage Vin is fixed at 58.8V with the MPPT method, the average value of current Iin is variable between 2.37A and 3.06A; as a result, the maximum power energy is variable between 139.35W(58.8V×2.37A) and 180W(58.8V×3.06A).

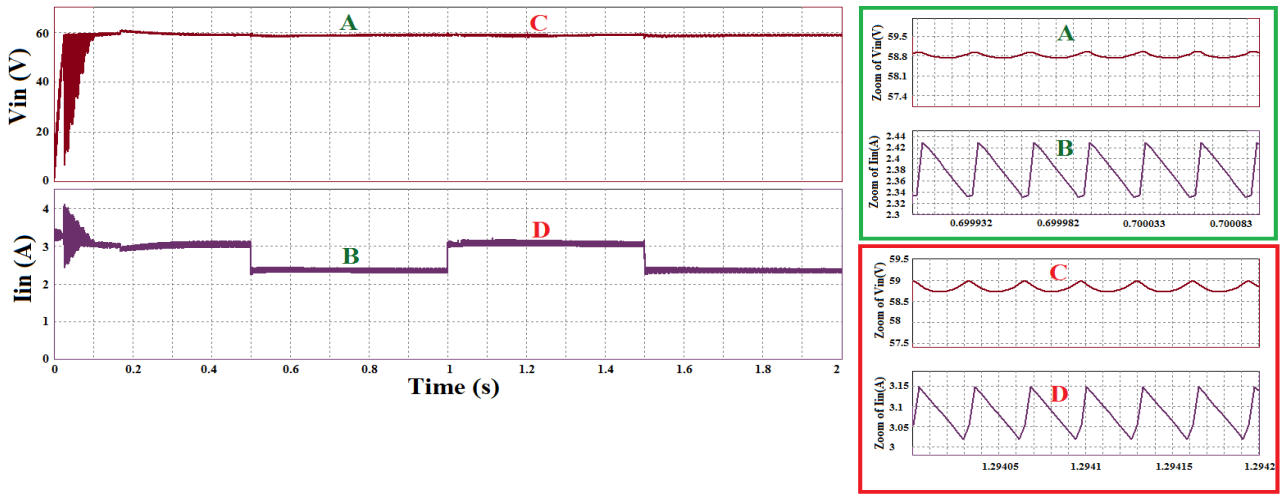


Fig. 13 The voltage Vin (V) and current Iin (A) supplied to the HSUC with the MPPT method

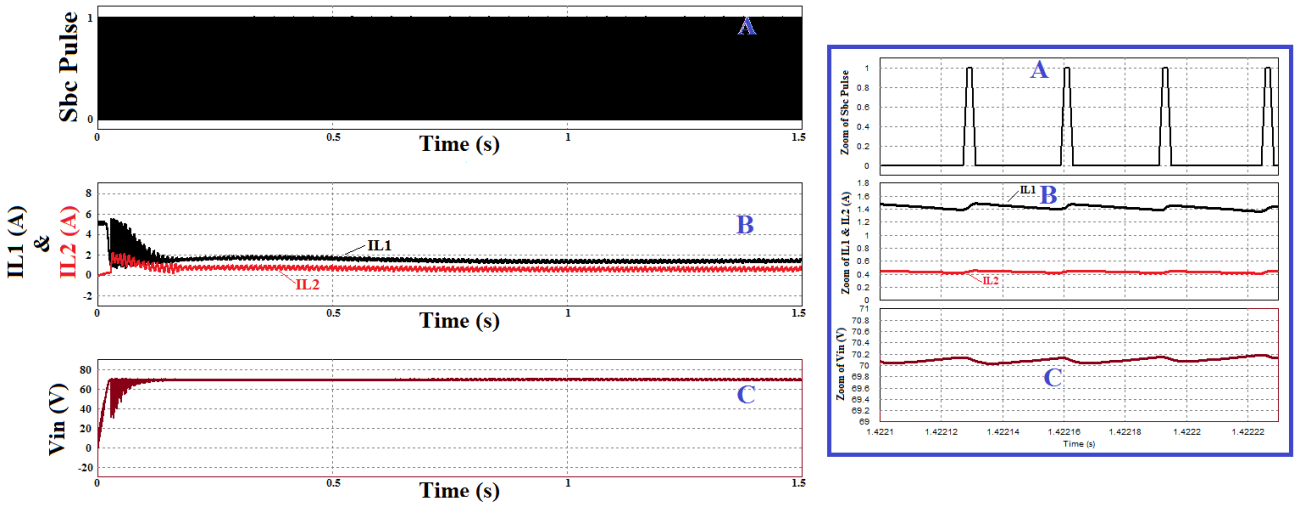
It's clear from the presented results that the used HSUC is apt to work with the MPPT method to extract maximum power energy from solar panels.

4.2. Simulation results of the studied photovoltaic multilevel inverter with PWM method (MI=0.92)

In order to test the influence of the PWM control method (Fig. 11) on the charging and discharging cycles of the used capacitors, the HSUC is controlled in open loop with a fixed pulse signal, and the DC-AC FLC is controlled with the PWM method with a fixed modulation index. The important used parameters in this simulation test are listed below:

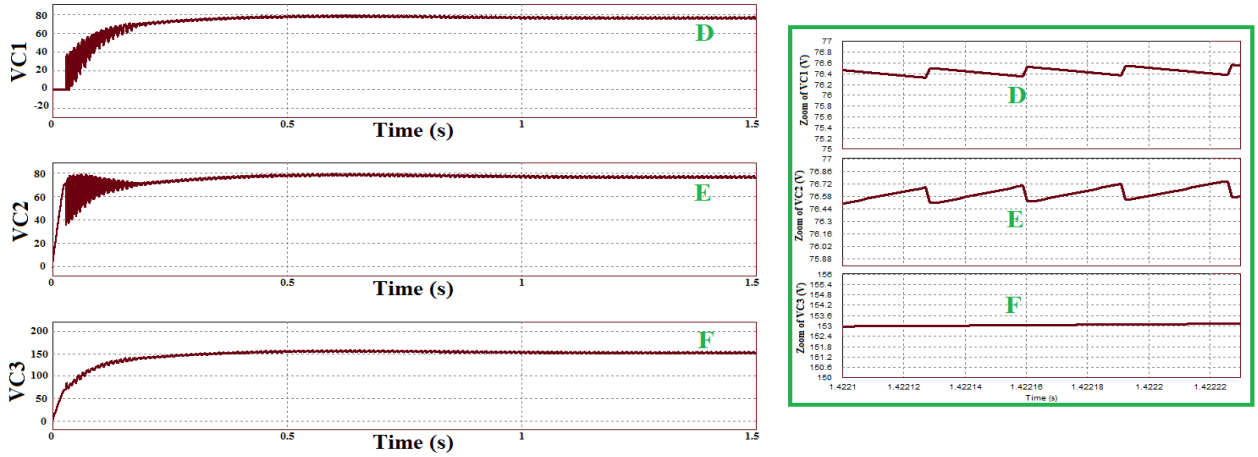
(1) The MI of the PWM method is 0.92.
(2) The value of D is 0.09.
(3) The frequency of the fixed pulse signal Fs is 31 kHz.
(4) The AC load is inductive: R=64.81Ω; L=0.488H; Cos (φ) =0.38.
(5) The irradiation level is 600W/m2 and the temperature level is 25°c.
(6) The frequency of the two identical carrier signals used in the PWM method is Fcarr= 2 kHz.

Fig. 14 presents an overview of the used pulse control signal, the charging and discharging currents of the inductors L1 and L2, the input voltage Vin from solar panels, the voltages across the capacitors C1, C2, C3, and Cbc, the voltage VDC-Bus, the obtained AC voltage and current, and the FFT spectrum.

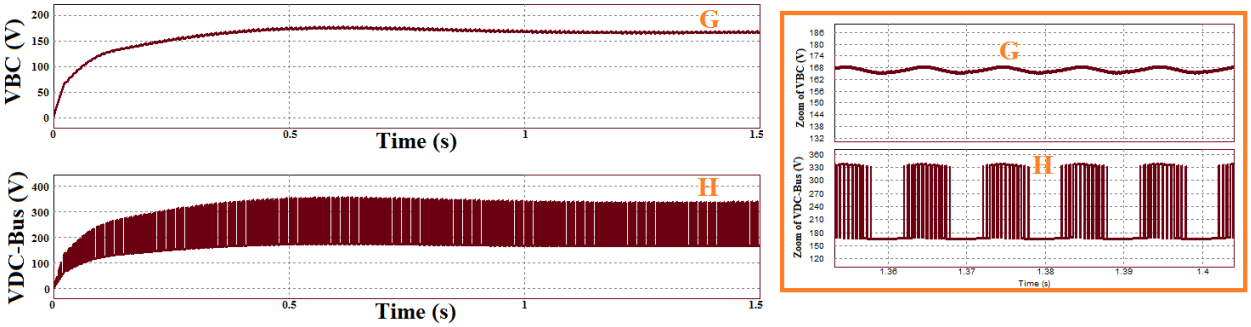


(a) A: Sbc Pulse; B: currents IL1and IL2; C: voltage Vin

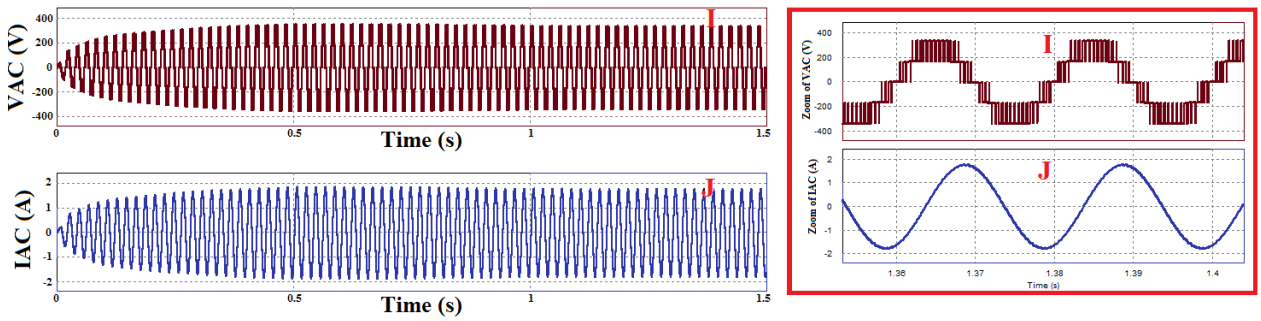
Fig. 14 Simulation results of the studied photovoltaic multilevel inverter with PWM method



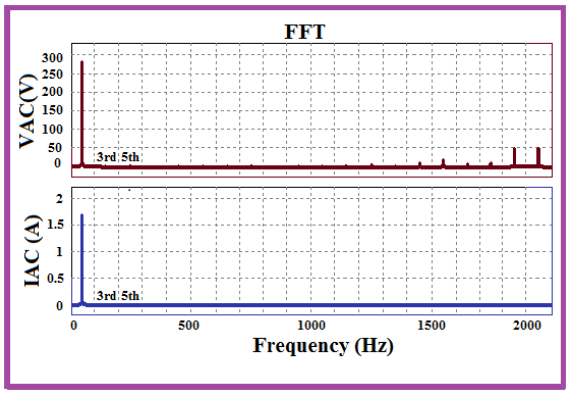
(b) D: voltage VC1; E: voltage VC2; F: voltage VC3



(c) G: voltage VBC; H: voltage VDC-Bus



(d) I: voltage VAC; J: current IAC



(e) K: FFT spectrum of VAC and IAC

Fig. 14 Simulation results of the studied photovoltaic multilevel inverter with PWM method (continued)

The two solar panels deliver an input DC voltage Vin of 70V (Fig. 14 (a)) to the PV system. The ripple of the current IL1 across the inductor L1 (2mH) is very small and the average value of this current is 1.45A (Fig. 14 (a)). The ripple of the current IL2 across the inductor L2 (12mH) is also very small and the average value of this current is 0.67A (Fig. 14 (a)). The ripple of the voltage VC1 across the capacitor C1 is very small and the average value of this voltage is 76V (Fig. 14 (b)). The ripple of the voltage VC2 across the capacitor C2 is very small and the average value of this voltage is 76V (Fig. 14 (b)).The ripple of

the voltage VC3 across the capacitor C3 is very small and the average value of this voltage is 153V (Fig. 14 (b)).The HSUC delivers an output voltage VBC of 167V (Fig. 14 (c)) by using the small duty cycle (0.09). The VDC-Bus voltage from the SCC (Fig. 14 (c)) starts from 167V and ends at 334V repeated at each half period (0.01s). The FBC delivers an output AC voltage (Fig. 14 (d)) with five levels and an RMS value of 219V. The output AC current (Fig. 14 (d)) is sinusoidal in shape with an RMS value of 1.26A. The FFT analysis of VAC and IAC (Fig. 14 (e)) shows that the even harmonics are absent and the first important odd harmonics (3rd, 5th) are absent.

It's clear from the obtained results that the proposed multilevel inverter converter is able to be controlled with the PWM method without any problem of voltage balancing across the used capacitors. Also with the proposed PWM method, this multilevel inverter delivers optimal AC voltage and current with fewer harmonics without using filters.

5. Experimental Results

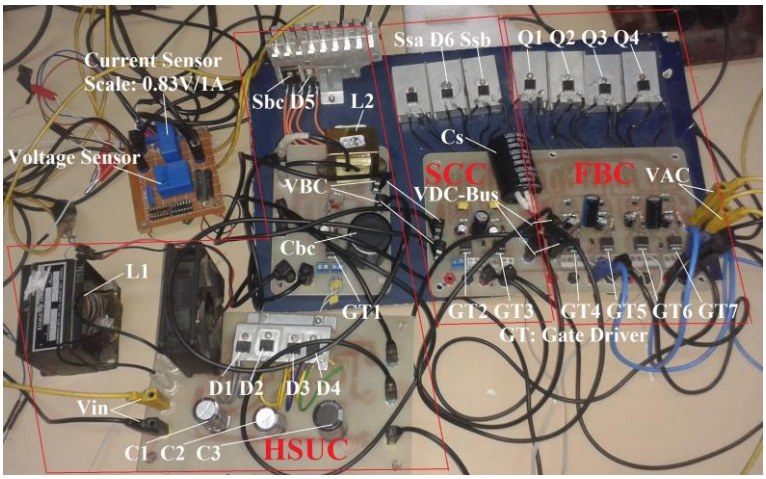


Fig. 15 The experimental prototype of the proposed multilevel inverter

An experimental prototype (200W rated power) of the proposed multilevel inverter is fabricated at the laboratory as shown in Fig. 15. The values of the main elements used experimentally are the same as indicated in Table 3. In order to record the experimental results a digital oscilloscope (DO) is used, it contains two channel for measuring (ch1 and ch4).

5.1. Experimental results of the used HSUC with MPPT

The MPPT method shown in Fig. 10 is implemented on a microcontroller and tested with the HSUC. Fig. 16 shows the synoptic of the experimental test bench. In order to respect the rated power (200W) of the fabricated HSUC, a variable DC source (0-63V/0-3A) is used as an input voltage for the experimental setup. The objective of this test is to adjust automatically the input voltage from the variable DC source at a chosen Vmpp-Ref and extract the maximum current (3A).

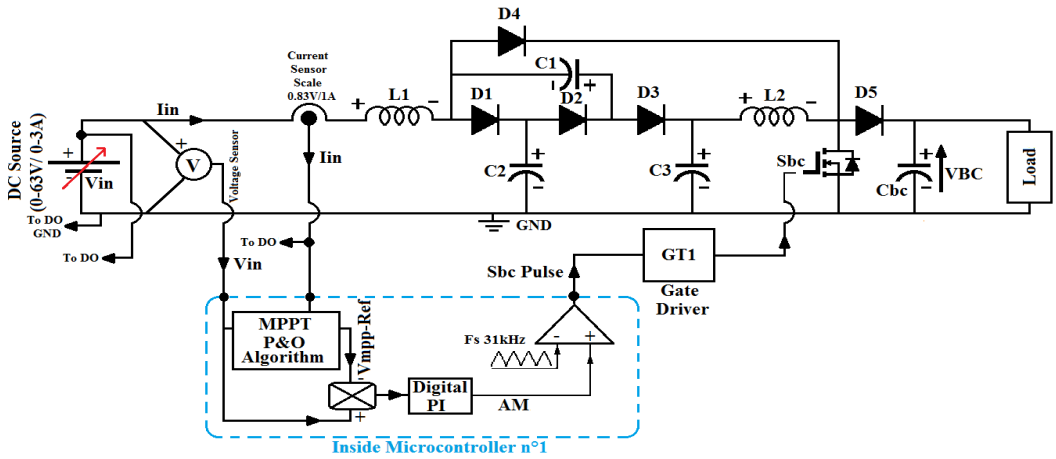


Fig. 16 Synoptic of the experimental test bench of the HSUC with the MPPT method

The important used parameters in this test are listed below:

(1) Vmpp-Ref of the MPPT is 59V.

(2) The value of Fs is 31 kHz.

(3) The output load is constant with a rated power of 200W.

(4) The used current sensor delivers 0.83V for each 1A.

Fig. 17 shows the regulated input voltage Vin with the delivered maximum current Iin from the variable DC source under MPPT test.

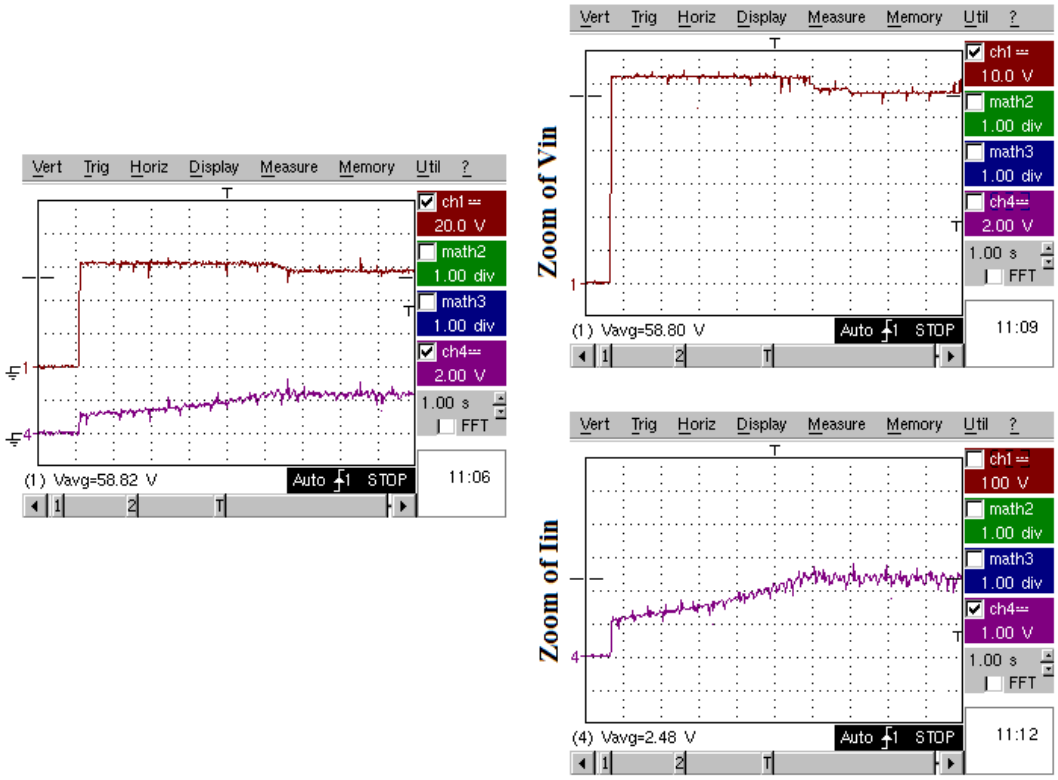


Fig. 17 The input voltage Vin (ch1) and input current Iin (ch4) under MPPT test

From Fig. 17, the input voltage Vin from variable DC source is regulated automatically at 58.8V (ch1), and the generated current Iin for the HSUC oscillates around 3A (ch4) (Pmax=176.4W); this proves the robustness of the implemented MPPT program, and also the ability of the HSUC to be used with critical MPPT methods.

5.2. *Experimental results of the studied photovoltaic multilevel inverter with PWM method* (*MI=0.92*)

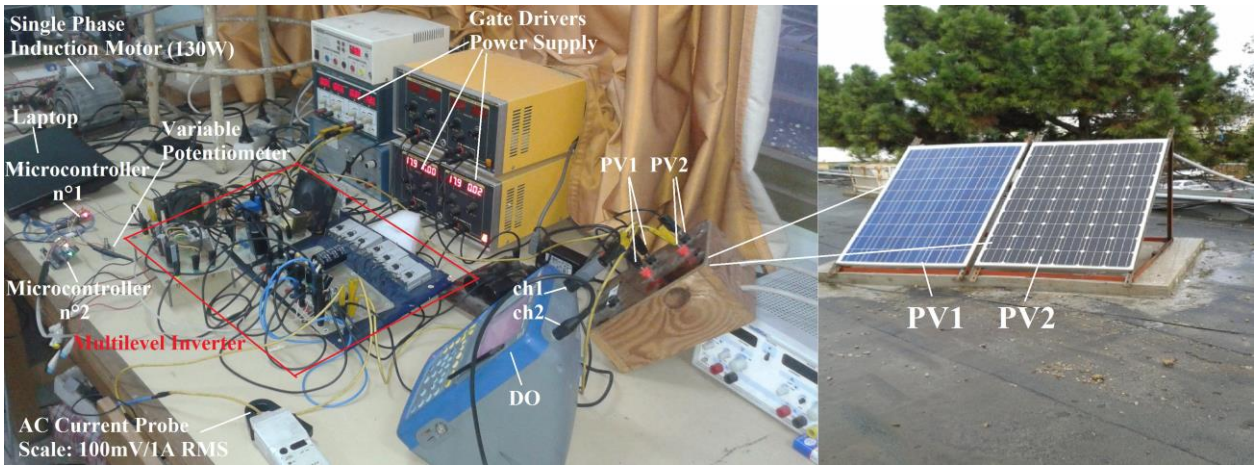


Fig. 18 the two solar panels installed at the laboratory roof with the experimental test bench

In this test, the HSUC is controlled in open loop with a variable pulse signal from a potentiometer, and the DC-AC FLC is controlled with the PWM method with a fixed modulation index (Fig. 11). Two solar panels coupled in series installed at the laboratory roof are used as a DC source for the experimental setup as shown in Fig. 18, which its characteristics are the same as indicated in Table 4. Fig. 19 shows the synoptic of the experimental test bench. Two microcontrollers are used as a digital control system. The switches Q2, Q3, Ssb, and Sbc have a common source with the GND for this; a common power supply for the gate drivers is used.

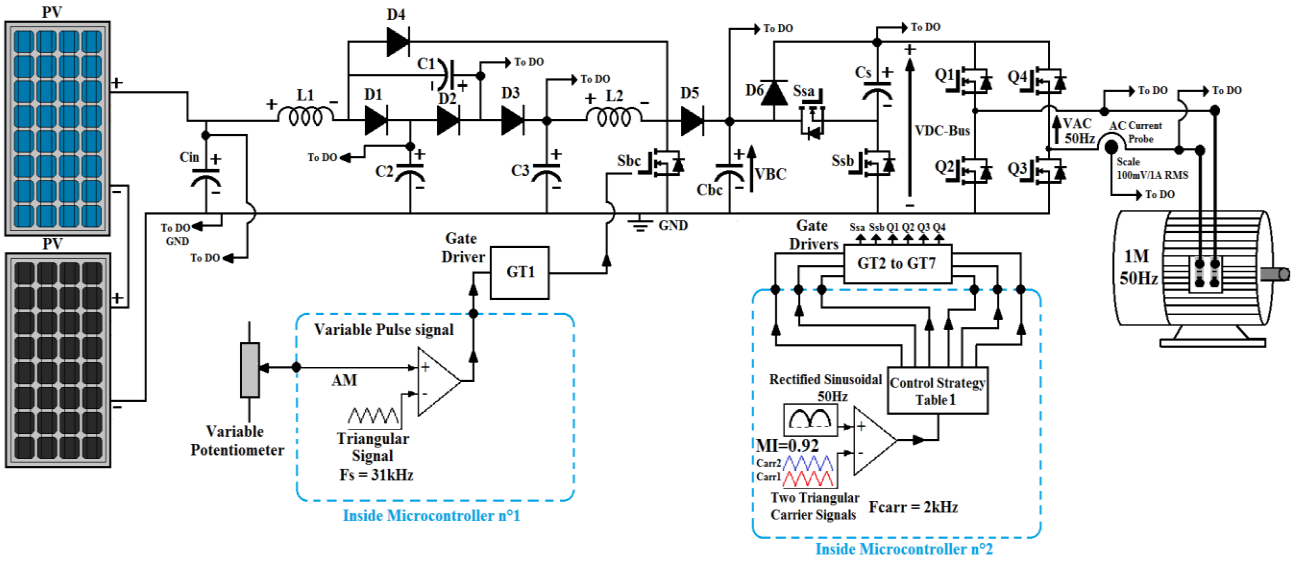
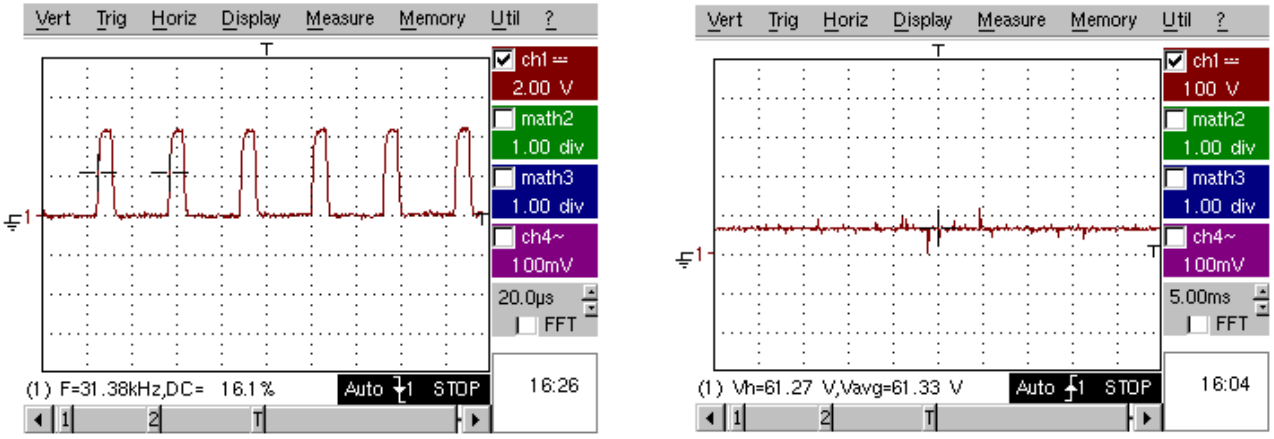


Fig. 19 Synoptic of the experimental test bench of the proposed multilevel inverter with PWM method

The important used parameters are:

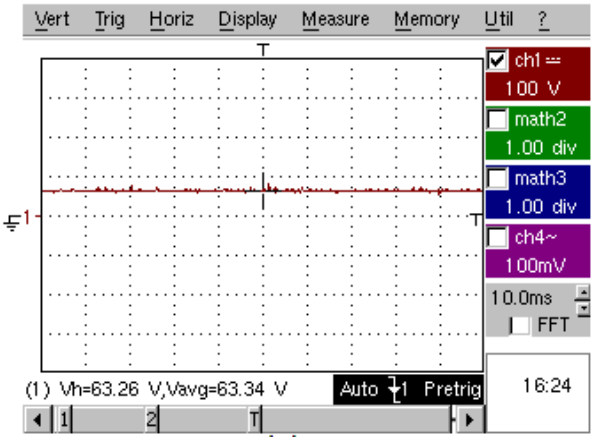
(1) The MI of the PWM method applied on the DC-AC FLC is 0.92.
(2) The value of Fs is 31 kHz.
(3) The frequency of the two identical carrier signals used in the PWM method is Fcarr= 2 kHz.
(4) The AC load is a 130W single phase induction motor.
(5) The used AC current probe delivers 100mV for each 1A RMS.

Fig. 20 presents an overview of the used pulse control signal, the input voltage Vin from solar panels, the voltages across the capacitors C1, C2, C3, and Cbc, the voltage VDC-Bus, the obtained AC voltage and current, and the FFT spectrum.

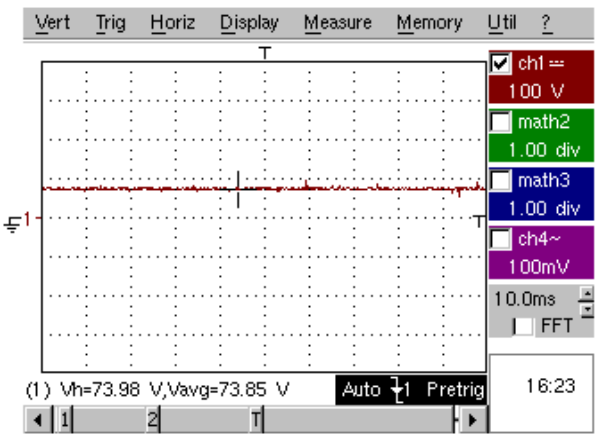


(a) Sbc Pulse (b) Voltage Vin

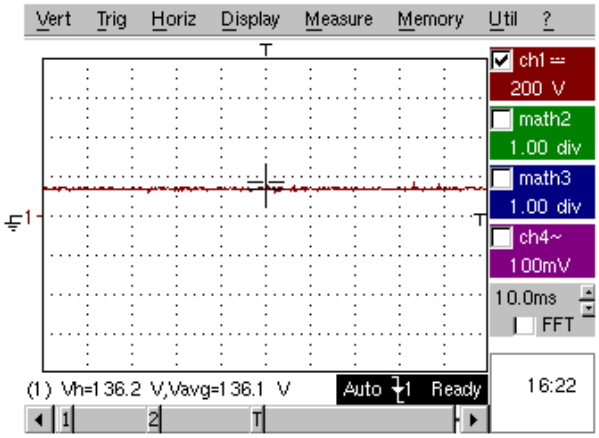
Fig. 20 Experimental results of the studied photovoltaic multilevel inverter with PWM method



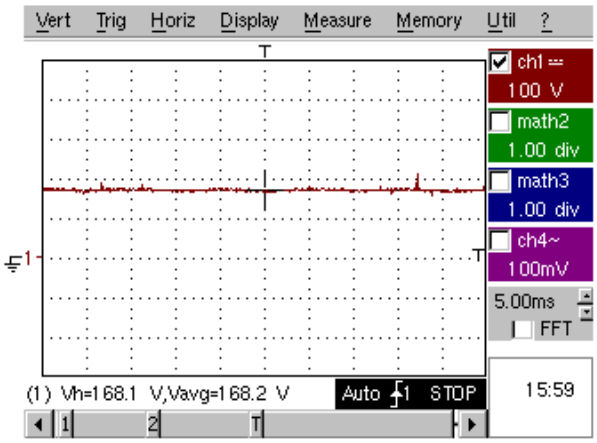
(c) Voltage VC1



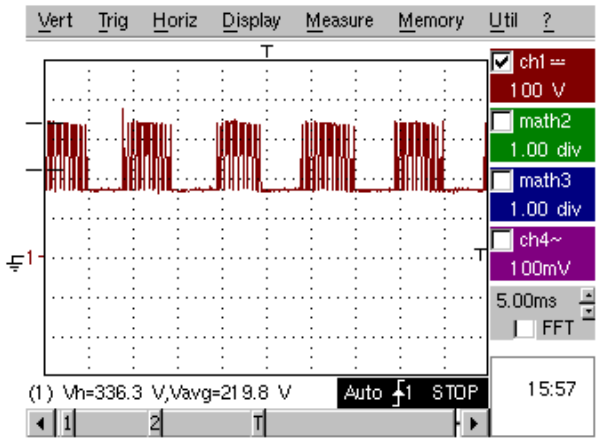
(d) Voltage VC2



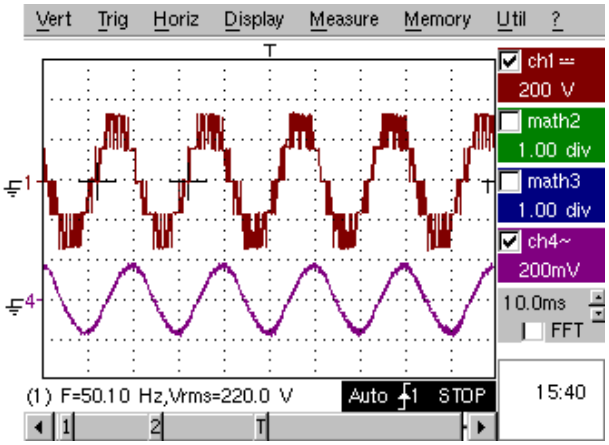
(e) Voltage VC3



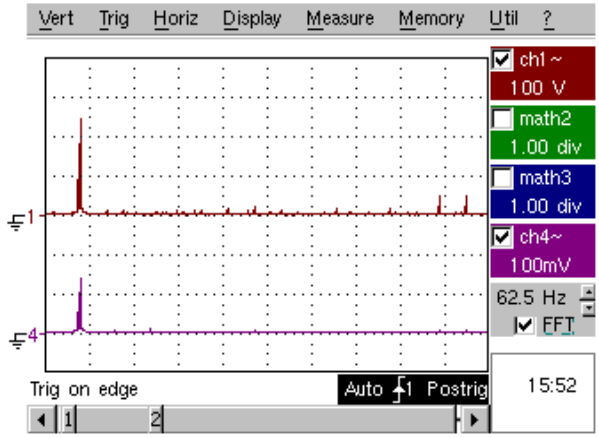
(f) Voltage VBC



(g) Voltage VDC-Bus



(h) Output AC voltage (ch1) and output AC current (ch4)



(i) FFT spectrum of VAC and IAC

Fig. 20 Experimental results of the studied photovoltaic multilevel inverter with PWM method (continued)

The two solar panels deliver an input DC voltage Vin of 61.33V (Fig. 20 (b)) to the experimental setup. The voltage VC1 across the capacitor C1 is constant with an average value of 63.34V (Fig. 20 (c)). The voltage VC2 across the capacitor C2 is constant with an average value of 73.85V (Fig. 20 (d)).The voltage VC3 across the capacitor C3 is constant with an average value of 136.1V (Fig. 20 (e)).The HSUC delivers an output voltage VBC of 168.2V (Fig. 20 (f)) by using a small duty cycle D of 0.16 (Fig. 20 (a)). The VDC-Bus voltage from the SCC (Fig. 20 (g)) starts from 168V and ends at 336.3V repeated at each half period (0.01s). The FBC delivers an output AC voltage (ch1) (Fig. 20 (h)) with five levels and an RMS value of 220.4V. The output AC current (ch4) (Fig. 20 (h)) is sinusoidal in shape with an RMS value of 1.22A. The FFT analysis of VAC and IAC (Fig. 20 (i)) shows that the even harmonics are absent and the first important odd harmonics (3rd, 5th) are absent.

The experimental results confirm that the photovoltaic multilevel inverter with the PWM method is apt to supply power energy from solar panels to industrial machines such as induction motors with no voltage balancing problem across capacitors. In addition, this inverter delivers good output AC waveforms with fewer harmonics without using output filter.

5.3. The voltage conversion ratio of the fabricated HSUC, and the efficiency of the proposed multilevel inverter:

(1) Voltage conversion ratio (G):

The voltage conversion ratio (G) of the fabricated HSUC has been compared experimentally to a conventional boost converter for different values of the duty cycle (D). Fig. 21 shows the obtained results.

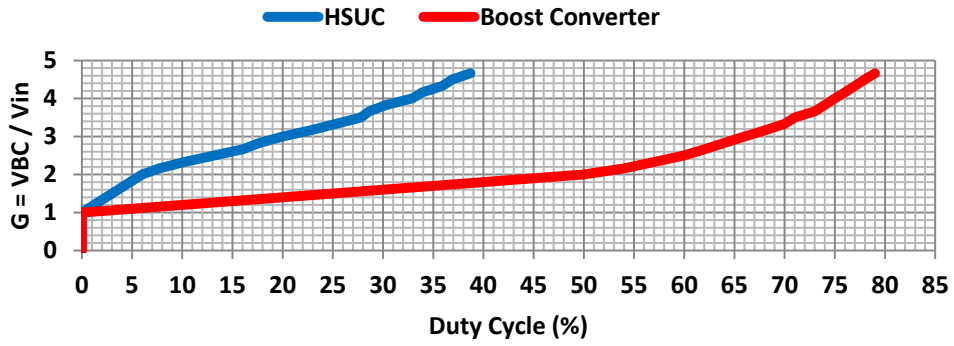


Fig. 21 The voltage conversion ratio of the HSUC and the conventional Boost Converter

From Fig. 21, the HSUC offers the possibility to transfer more energy with high voltage using just a small duty cycle compared to the classical Boost Converter.

(2) The efficiency of the proposed inverter:

The efficiency of the HSUC and the DC-AC FLC circuits has been analyzed experimentally for different levels of power energy. Fig. 22 shows the obtained results.

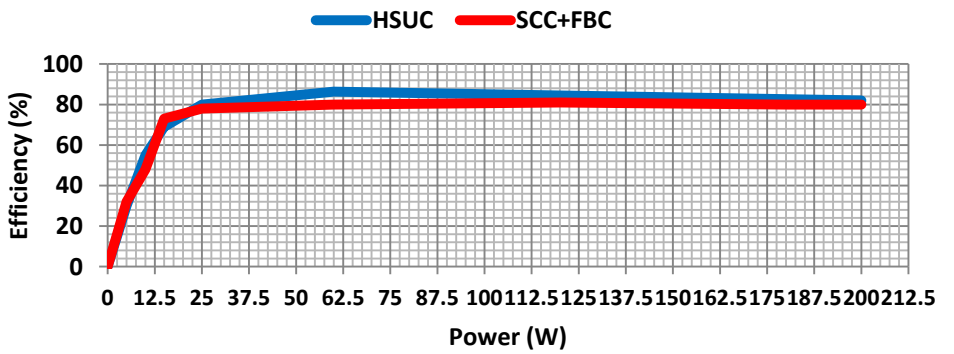


Fig. 22 The efficiency of the HSUC and the DC-AC FLC circuits

From Fig. 22, the efficiency of the HSUC circuit and the DC-AC FLC circuit is around 80%. This percentage has been obtained from the first experimental test at the laboratory, but it will be increased using other optimal power switches.

6. Conclusions

In this paper, a new single-phase five-level inverter for PV system applications has been proposed. This multilevel inverter was novel, because it combined an HSUC converter recently presented in the literature with an efficient DC-DC SCC and a simple H-bridge DC-AC converter. To generate five-level output AC voltage, the proposed topology requires only a single input DC voltage source from solar panels in contrast to conventional multilevel inverters. The maximum power point method and PWM technique were used for testing in simulations and experiments with a 200 W prototype. The transfer of power energy from solar panels to the AC load with this inverter was performed using a small duty cycle (< 0.2) of the control signal for the DC-DC converter.

This multilevel inverter presents many advantages, such as reduced number of power switches (seven) and gate driver power supply, good output AC waveforms, fewer harmonics, no voltage balancing problem across capacitors, low switching losses, high efficiency, the ability to extract maximum power energy from solar panels, the ability to supply power energy from a low-voltage DC source to industrial machines meeting industrial criteria for voltage and frequency (220 V; 50 Hz), simplicity, and easy implementation. For all these reasons, the proposed system can be used as an alternative type of inverter in PV system applications.

In future work, the performance of the proposed PV multilevel inverter will be ameliorated by increasing its rated power (1 KW) and using a closed loop control system.

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