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Analysis of Drain-Induced Barrier Lowering for Gate-All-Around FET with Ferroelectric

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Abstract

This study presents an analytical model for the drain-induced barrier lowering (DIBL) of a junctionless gate-all-around FET with ferroelectric, utilizing a 2D potential model. A multilayer structure of metal-ferroelectric-metal-insulator-semiconductor is used as the gate, as well as the remanent polarization and coercive field values corresponding to HZO are used. The DIBLs obtained with the proposed model demonstrate good agreement with those obtained using the second derivative method, which relies on the 2D relationship between drain current and gate voltage. The results demonstrate that an increase in ferroelectric thickness leads to a negative DIBL value due to the ferroelectric charge. Additionally, there exists an inverse relationship between ferroelectric thickness and channel length to achieve a DIBL value of 0. This condition is satisfied only with the increase of the ferroelectric thickness as the channel radius and insulator thickness increase. The DIBLs increase with higher remanent polarization and lower coercive field, remaining constant when the ratio of remanent polarization and coercive field is maintained.

Keywords: gate-all-around, DIBL, ferroelectric, remanent polarization, coercive field

1. Introduction

The short channel effects, caused by the reduction in transistor size, are reaching a stage where the transistor performance can no longer be guaranteed. In particular, the urgent problem to be addressed is the increase in power dissipation resulting from the decrease in transistor size. To solve this problem, active research is being conducted on negative capacitance field-effect transistor (NCFET) using a ferroelectric, which can reduce the parasitic current in the subthreshold region [1-3].

It is known that the subthreshold swing (SS) can be reduced to less than 60 mV/dec by exploiting the relationship between polarization and field within the ferroelectric when the ferroelectric is stacked with SiO_2 as a gate oxide. As a result, the NCFETs solve the Boltzmann limit, thereby rapidly reducing the parasitic current [4-5]. In the case of these NCFETs, the threshold voltage changes according to the ferroelectric's thickness. Therefore, stabilizing the threshold voltage according to the drain voltage change becomes a problem. Additionally, in the case of NCFETs, a phenomenon known as drain-induced barrier rising (DIBR) occurs rather than the drain-induced barrier lowering (DIBL) phenomenon. Unlike the conventional MOSFET, where an increase in drain voltage decreases the threshold voltage, in NCFETs, the threshold voltage exhibits an increase.

The DIBR phenomenon is caused by the charge change in the ferroelectric according to the drain voltage, and it is known to change according to the ferroelectric thickness [6-7]. Ongoing research is being conducted to identify this phenomenon in planar-type MOSFETs, double-gate MOSFETs, and FinFETs [8-10]. However, there has been limited research on the DIBR

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phenomenon in the gate-all-around (GAA) field-effect transistor (FET), which is considered the ultimate FET structure. Many experiments have demonstrated the DIBR phenomenon of GAA FET, making theoretical investigation urgent. Therefore, the DIBL phenomenon of GAA FET will be analyzed in this paper.

Rassekh et al. [11] theoretically presented the DIBR phenomenon of a double gate (DG) NCFET using potential distributions approximated by parabolic curves. Awadhiya et al. [12] analyzed the threshold voltage and DIBL when a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) was used in the gate structure of a conventional FET rather than a GAA FET or DG MOSFET. Saha et al. [13] described a negative DIBL using metal-ferroelectric-insulator-semiconductor (MFIS) for DG MOSFET using 2D Poission's equation and Green's function, and Chaudhary et al. [14] analyzed DIBL with Silvaco TCAD using MFMIS structures over fully-depleted silicon-on-insulator (FDSOI).

In addition, Lee et al. [15-16] experimentally investigated that DIBL was negative, showing a value of SS < 60 mV/dec for the GAA FET with the MFMIS gate oxide structure using the ferroelectric of HfZrO (HZO). In particular, Lee et al. [15-16] tested the advantages of using the MFMIS structure rather than the MFIS structure, such as decreased SS in the subthreshold region and increased current in the on-state. In a review paper by Qin et al. [17], despite the greater complexity of the process involved in the MFMIS structure compared to the MFIS structure, it is pointed out that the SS is reduced and the on-current is improved by the inner gate voltage amplification effect. Therefore, the DIBL for GAA FET with MFMIS structure will be analyzed in this paper.

To this end, an analytical DIBL model obtained using the 2D solution of Poisson's equation will be presented and the validity of this model will be demonstrated. In particular, a junctionless channel structure developed to simplify the process according to the decrease in channel length will be used, and HZO will be used as the ferroelectric material [18-19]. Since the remanent polarization P_r and coercive field E_c of HZO are the main factors determining the NC, the effect of these two factors on DIBL will be considered.

2. DIBL of MFMIS Junctionless GAA FET with Ferroelectric

This section describes the structure of the GAA FET with ferroelectric and the mathematical model for analyzing DIBL. The validity of the model will be demonstrated by comparing the DIBLs obtained through the proposed mathematical model and those derived from the current-voltage characteristics obtained using 2D potential distribution. Additionally, the cause of the DIBR phenomenon will be explained using a ferroelectric charge.

2.1. Structure of junctionless GAA FET with ferroelectric and analytical DIBL model

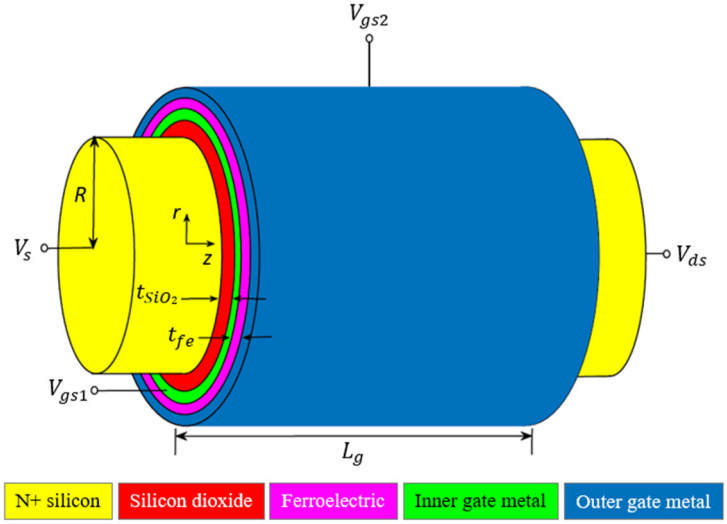


Fig. 1 Schematic view of junctionless GAA FET with MFMIS structure

The ferroelectric junctionless GAA FET used in this paper is shown in Fig. 1, and the device parameters are shown in Table 1. V_{gs1} is the voltage induced to the inner gate metal, and V_{gs2} is the voltage applied to the outer gate metal. To obtain the potential distribution within the channel of a MOSFET with a GAA structure, the 2D potential model for the r and z directions presented by Li et al. [20] was used.

Table 1 Device parameters for this analytical SS model

Device parameter	Symbol	Value
Channel length	L_g	15-100 nm
Channel radius	R	3-7 nm
SiO_2 thickness	t_{ox}	1-3 nm
Doping concentration	N_d	10^{18} /cm^3
Ferroelectric thickness	t_{fe}	0-10 nm
Remanent polarization	P_r	5-20 μC/cm^2
Coercive field	E_c	0.5-1.5 MV/cm

In other words, the potential in the channel can be obtained by the formula below, which is the sum of the 1D solution $\phi_1(r)$ of Poisson's equation and the 2D solution $\phi_2(r,z)$ of the homogeneous Laplace equation.

$$\phi(r,z)=\phi_1(r)+\phi_2(r,z) \tag{1}$$

$$\phi_1(r)=-\frac{qN_d}{4\varepsilon_{si}}r^2+V_{gs}-\phi_{ms}+\frac{qN_dR}{2C_{ox}}+\frac{qN_dR^2}{4\varepsilon_{si}} \tag{2}$$

$$\phi_2(r,z)=\sum_{n=1}^{\infty}\left[C_n\exp\left(\frac{\alpha_n z}{R}\right)+D_n\exp\left(-\frac{\alpha_n z}{R}\right)\right]J_0\left(\frac{\alpha_n r}{R}\right) \tag{3}$$

where the α_n is an eigenvalue satisfying the following equation:

$$RJ_0(\alpha_n)-\frac{\varepsilon_{si}}{C_{ox}}\alpha_n J_1(\alpha_n)=0 \tag{4}$$

The C_n and D_n are shown in Li's model [20].

To obtain the charge Q in the ferroelectric, the charge Q_{sc} in the channel must first be obtained from the relational expression:

$$Q_{sc}=-C_{ox}\left(V_{gs1}-\phi_{ms}-\phi_s\right) \tag{5}$$

At this time, the surface potential ϕ_s is the sum of $\phi_1(R)$ and $\phi_2(R,z)$ obtained by substituting $r=R$ into Eqs. (2) and (3), and by substituting them into Eq. (5), the charge Q_{sc} in the channel can be obtained as in the following:

$$Q_{sc}=C_{ox}\left\{\frac{qN_dR}{2C_{ox}}+\sum_{n=1}^{\infty}\left[C_n\exp\left(\frac{\alpha_n z}{R}\right)+D_n\exp\left(-\frac{\alpha_n z}{R}\right)\right]J_0(\alpha_n)\right\} \tag{6}$$

By substituting the expression from Eq. (6) into the formula below, Q can be obtained.

$$2\pi RL_g\times Q=-\int_0^{L_g}\pi RQ_{sc}dz \tag{7}$$

Here, Q_{sc} represents the charge in the channel per unit projected surface, so πR was used for the width in the GAA FET [21]. That is, Q is

$$\begin{aligned}Q&=-\frac{1}{2L_g}\int_0^{L_g}Q_{sc}dz\\&=-\frac{qN_dR}{4}-\frac{C_{ox}}{2L_g}\left\{\sum_{n=1}^{\infty}\left[C_n\exp\left(\frac{\alpha_nL_g}{R}\right)-D_n\exp\left(-\frac{\alpha_nL_g}{R}\right)-C_n+D_n\right]\left(\frac{R}{\alpha_n}\right)J_0(\alpha_n)\right\}\end{aligned} \tag{8}$$

and using Q, the ferroelectric voltage V_{fe} can be obtained as shown in the formula below, according to Landau theory [22].

$$V_{fe} = 2\alpha t_{fe} Q + 4\beta t_{fe} Q^3 + 6\gamma t_{fe} Q^5,\ \alpha = -\frac{3\sqrt{3}}{4}\frac{E_c}{P_r}(m/F);\ \beta = \frac{3\sqrt{3}}{8}\frac{E_c}{P_r^3}(m^5/F/C^2);\ \gamma = 0 \tag{9}$$

The threshold voltage of the outer gate metal in Fig. 1 has the following relationship with the threshold voltage of the inner gate metal.

$$V_{th2} = V_{fe} + V_{th1} \tag{10}$$

By the definition of DIBL, the DIBL can be expressed below,

$$DIBL = -\frac{dV_{th2}}{dV_{ds}} = -\frac{dV_{fe}}{dV_{ds}} - \frac{dV_{th1}}{dV_{ds}} \tag{11}$$

The second term from the right in Eq. (11) was obtained from the previous paper [23]. Therefore, the following formula for DIBL is obtained from Eq. (9).

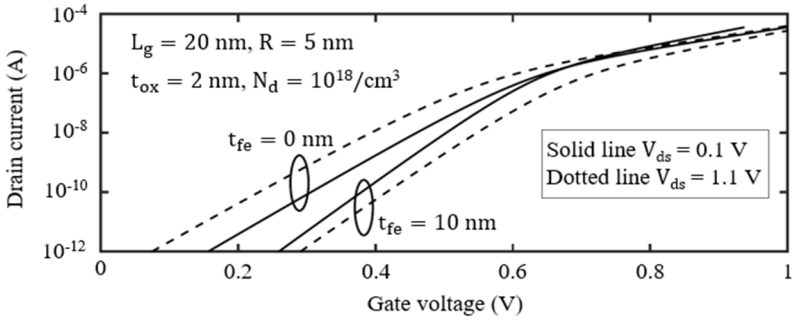
$$DIBL = \left(-2\alpha t_{fe} - 12\beta t_{fe} Q^2\right)\frac{dQ}{dV_{ds}} - \frac{dV_{th1}}{dV_{ds}} \tag{12}$$

In Eq. (12), dQ/dV_{ds} is

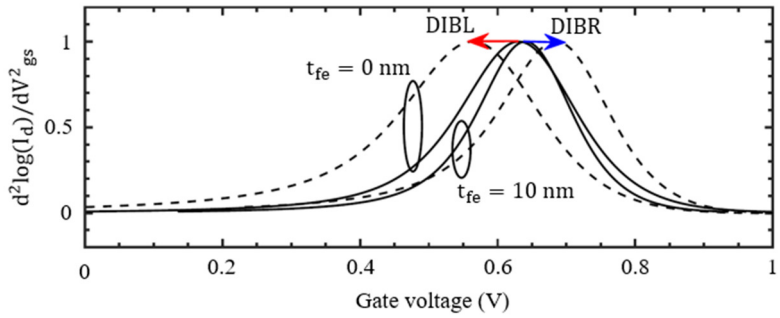
$$\frac{dQ}{dV_{ds}} = \sum_{n=1}^{\infty}\left(\frac{C_{ox}RJ_0(\alpha_n)}{2\alpha_n L_g}\right)\left(\frac{S_0}{2\sinh(-\alpha_n L_g/R)}\right)\left\{2 - \exp\left(\alpha_n L_g/R\right) - \exp\left(-\alpha_n L_g/R\right)\right\} \tag{13}$$

Therefore, the DIBL can be obtained analytically by substituting Eq. (13) into Eq. (12). The above equations were coded using MATLAB and the results were plotted. Here, S_0 is indicated in Li's model [20] and was calculated using only $n = 1$ due to the nature of the Fourier-Bessel series of Eq. (13).

2.2. *Comparison with DIBL derived from 2D potential distribution*



(a) Relation of drain current and gate voltage



(b) Threshold voltage shifts derived from the second derivative method

Fig. 2 Current-voltage characteristics and DIBL obtained using 2D potential distribution

To validate the analytical DIBL model presented in this paper, the DIBL was derived from the change in threshold voltage obtained from the relationship between drain current I_{ds} and gate voltage V_{gs} [23] using the 2D potential distribution. Fig. 2 shows the current-voltage characteristics and changes in threshold voltage for t_{fe} = 0 nm and t_{fe} = 10 nm under the given device parameters. The threshold voltage was obtained by the second derivative method [24]. As shown in Fig. 2, the threshold voltage decreases when the drain voltage increases at t_{fe} = 0 nm, but the threshold voltage increases as the drain voltage increases at t_{fe} = 10 nm. It can observed that a negative DIBL or DIBR value appears at t_{fe} = 10 nm.

In Fig. 3, the DIBL values derived from the I_{ds}–V_{gs} relationship, obtained using the 2D potential distribution, are compared with those obtained using the analytical DIBL model presented in this paper. The DIBL value obtained from the I_{ds}–V_{gs} relationship derived from the 2D potential distribution and the analytical model show good agreement. Therefore, the DIBL of junctionless GAA FET with ferroelectric will be analyzed using the analytical DIBL model in this paper.

The presence of ferroelectric results in negative DIBL values. With the increase of ferroelectric thickness, the DIBL gradually decreases [14]. For t_{fe} = 10 nm, the DIBL value is negative in the entire channel length range of 15 nm to 100 nm under the given device parameters. For t_{fe} = 0 nm, the DIBL decreases as the channel length increases, but when t_{fe} increases, the DIBL decreases and then increases as the channel length increases.

To compare with the case of the DG MOSFET, the DIBL of the DG MOSFET is shown as a dotted line in Fig. 3 [25]. It can be observed that the change in DIBL according to ferroelectric thickness is more severe than that of GAA FET. At a ferroelectric thickness of 10 nm, DIBL tends to decrease and then increase as the channel length increases, similar to the GAA FET.

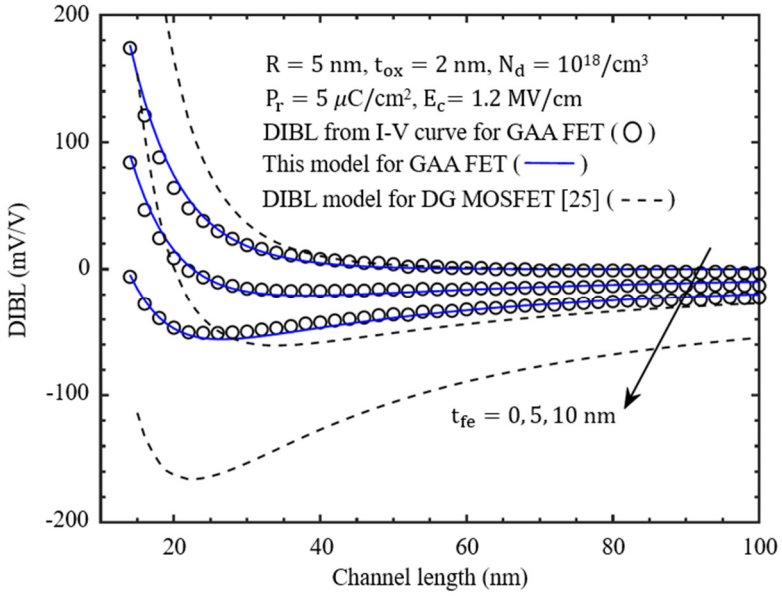
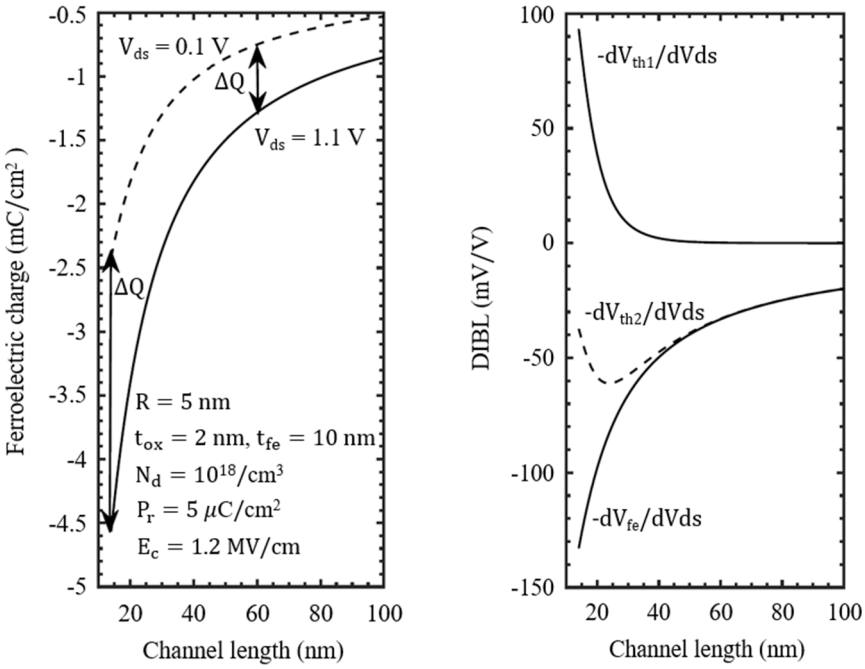


Fig. 3 Comparisons of the DIBLs derived from the 2D potential distribution and the proposed analytical model of GAA and DG MOSFET [25]

To analyze this phenomenon, the change in ferroelectric charge according to the channel length is shown in Fig. 4(a) with the drain voltage as a parameter. As shown in Fig. 4(a), since it is the case of ΔV_{ds} = 1 V, it can be expressed as $\Delta Q / \Delta V_{ds} = \Delta Q$ [C/V-cm^2]. In other words, it can observed that ΔQ increases as the channel length becomes shorter, as shown in Fig. 4(a).

Therefore, as shown in Fig. 4(b), $-dV_{fe} / dV_{ds}$ decreases significantly as the channel length decreases. At this time, when it is added to $-dV_{th1} / dV_{ds}$, which is the DIBL of the inner gate metal, it can be observed that the DIBL changes according to the channel length in the form of the dotted line in Fig. 4(b). In the end, it can be observed that the DIBL of the junctionless GAA FET with ferroelectric greatly depends on $-dV_{fe} / dV_{ds}$.



(a) Ferroelectric charges for channel length (b) DIBLs for channel length

Fig. 4 Relationship of ferroelectric charges and DIBL for channel length

3. DIBL of Junctionless GAA FET with Ferroelectric

In this section, the changes in DIBL will be explained using the analytical DIBL model for the ferroelectric characteristics and device parameters of the GAA FET, as shown in Table 1. In particular, the device parameters to achieve an ideal DIBL value of 0 mV/V will be obtained.

3.1. DIBL for device parameters

As shown in Fig. 3, the change of DIBL according to the ferroelectric thickness did not demonstrate a constant trend. A contour plot in Fig. 5 illustrates the variation of DIBL with the change in the ferroelectric thickness and channel length. As shown in Fig. 5, the changing trend of DIBL did not demonstrate a constant trend at the given ferroelectric thickness and channel length, and the most interesting line of DIBL = 0 mV/V showed an inverse relationship between the ferroelectric thickness and channel length.

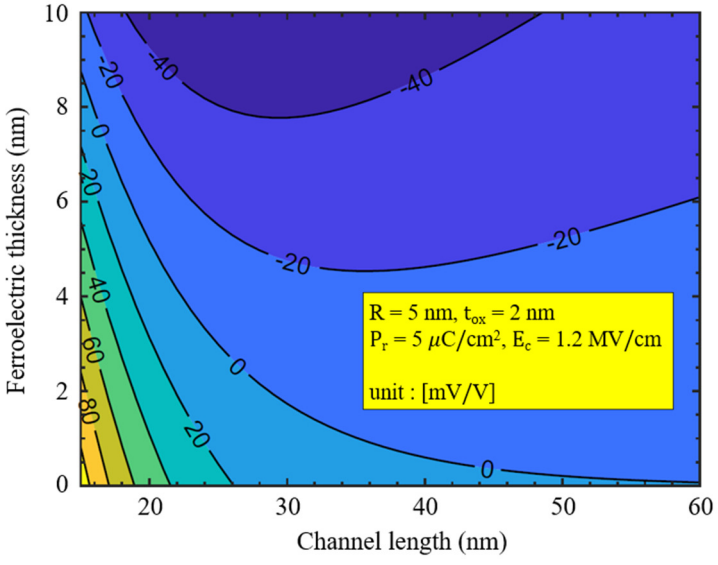


Fig. 5 Contours of DIBL for the ferroelectric thickness and channel length

In the region exhibiting positive DIBL, the changes in DIBL maintain an inversely proportional relationship between ferroelectric thickness and channel length to keep DIBL constant. However, it is observed that the inverse relationship does not hold in the negative DIBL region. As the ferroelectric thickness decreases, the ferroelectric charge will decrease and its effect on DIBL will decrease. Therefore, when the ferroelectric thickness is small, positive DIBL will appear regardless of the channel length, as the effect of $-dV_{fe}/dV_{ds}$ in Eq. (11) is minimal. Therefore, DIBL will increase as the channel length decreases.

However, when the ferroelectric thickness increases to 10 nm, as shown in Fig. 4, a phenomenon resulting from a rapid increase in $|\Delta Q|$ appears, and the effect of $-dV_{fe}/dV_{ds}$ cannot be ignored. Therefore, a negative DIBL phenomenon appears. In addition, as the ferroelectric thickness and channel length decrease, the DIBL changes rapidly, and as the channel length increases, the change in DIBL decreases.

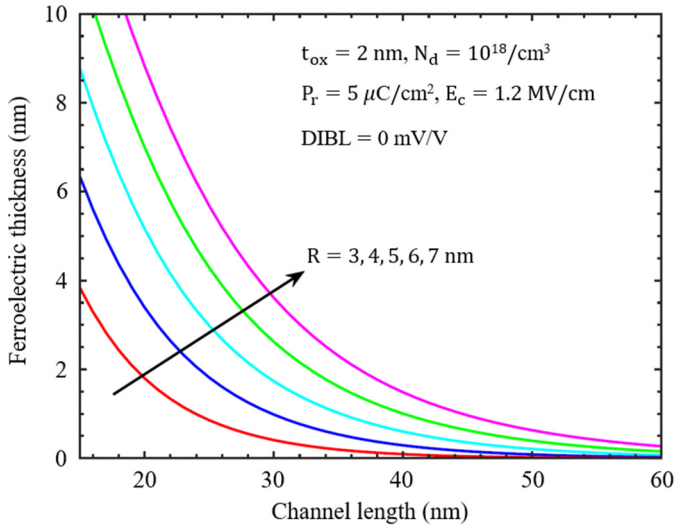


Fig. 6 Contours of DIBL = 0 mV/V with the silicon radius as a parameter

As illustrated in Fig. 5, achieving the ideal characteristics of DIBL = 0 mV/V in GAA FET with ferroelectric can be obtained by adjusting the ferroelectric thickness and channel length, as DIBL has negative and positive values. In Fig. 6, a line corresponding to DIBL = 0 mV/V, with the channel radius R as a parameter, is shown for the change of ferroelectric thickness and channel length. In Fig. 5, the lower part of the line corresponds to the region where DIBL > 0 mV/V, while the upper part represents the area of DIBL < 0 mV/V. As shown in Fig. 6, when R increases, the ferroelectric thickness and channel length must also increase to satisfy the condition of DIBL = 0 mV/V due to scaling theory. Therefore, it can be seen that as R increases, the region of DIBL < 0 mV/V decreases in the range of calculated channel length and ferroelectric thickness.

To satisfy the condition of DIBL = 0 mV/dec, when the channel length is small, the ferroelectric thickness changes greatly with the change of the channel radius R. Conversely, when the channel length is long, the channel radius R has a minimal effect. However, the ferroelectric thickness must be very thin. In the end, for larger channel lengths, there may be no necessity to use ferroelectric to satisfy DIBL = 0 mV/V. Conversely, for shorter channel lengths, the ferroelectric thickness must also increase according to R to satisfy the condition of DIBL = 0 mV/V.

Among the device parameters, the contour line of DIBL = 0 mV/V according to the thickness of SiO_2 used as an insulator in the MFMIS structure is shown in Fig. 7. As the oxide thickness increased, the area of DIBL < 0 mV/V decreased, and as the oxide thickness decreased to t_{ox} = 1 nm, it was observed that the area of DIBL < 0 mV/V greatly expanded in the range of calculated channel length and ferroelectric thickness. As demonstrated in the previously published paper [9], the absolute value of ΔQ decreases as the thickness of SiO_2 increases. Consequently, the absolute value of the first term on the right side of Eq. (12) decreases with increasing thickness of SiO_2. Therefore, DIBL increases as the thickness of SiO_2 increases. In addition, when the channel length is decreased, the DIBL = 0 mV/V line according to the oxide thickness is greatly affected by the

ferroelectric thickness. However, when the channel length is increased, the oxide thickness is hardly affected. Notably, if the oxide thickness increases, the ferroelectric thickness must also increase to satisfy the condition of DIBL = 0 mV/V due to scaling theory.

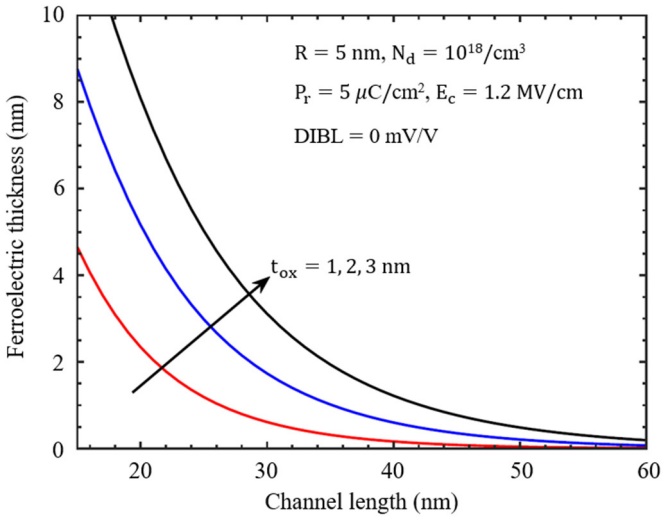
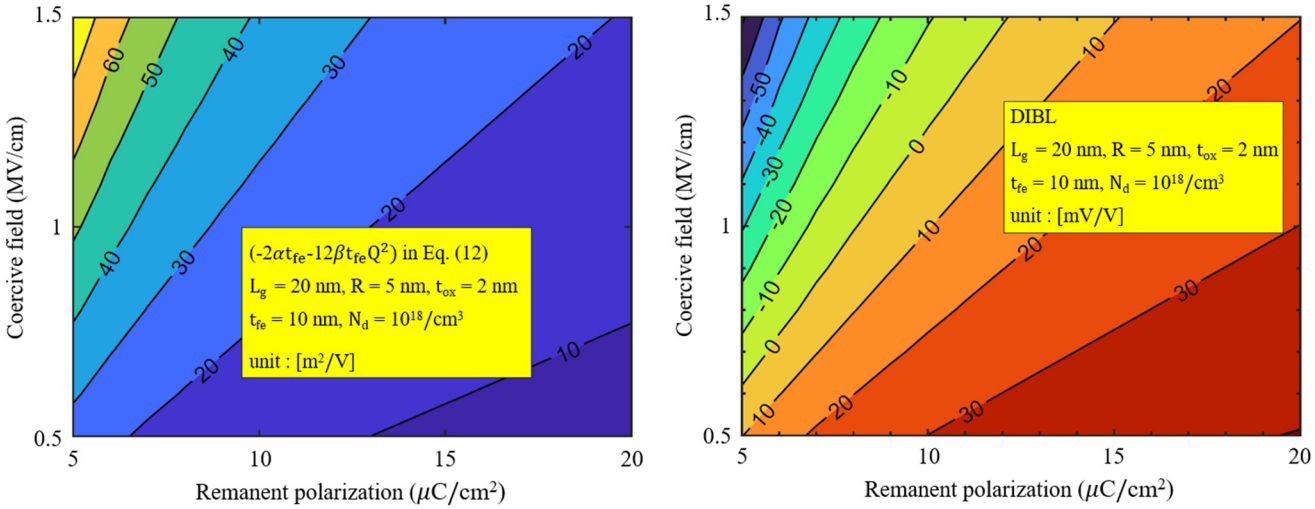


Fig. 7 Contours of DIBL=0 mV/V with the oxide thickness as a parameter

3.2. *DIBL for the parameters of ferroelectric*

In ferroelectric, the shape of the hysteresis curve is determined according to the remanent polarization P_r and the coercive field E_c, which has a great influence on characteristics such as SS [26-27]. In addition, since remanent polarization P_r and coercive field E_c affect the current-voltage characteristics of FET using ferroelectric, they will eventually affect DIBL. Therefore, the change of DIBL is analyzed for the change of remanent polarization P_r and coercive field E_c.

Fig. 8 shows the contour plots of the value of parentheses of Eq. (12) and DIBL for the change of remanent polarization P_r and coercive field E_c under the device parameters given in the figure. As the device parameters given in the figure are constant, both dQ / dV_{ds} and $-dV_{th1} / dV_{ds}$ maintain constant values, and the DIBL will only change depending on the change in the α and β values in parentheses in Eq. (12).



(a) Contours of the value of parentheses in Eq. (12) (b) Contours of DIBL

Fig. 8 Contours of parentheses in Eq. (12) and DIBL for the remanent polarization and coercive field

Comparing Figs. 8(a) and 8(b), it can be observed that DIBL decreases when the value of parentheses of Eq. (12) increases, as dQ / dV_{ds} is negative. As shown in Fig. 8(b), the DIBL shows a large change for the change of remanent polarization P_r and coercive field E_c, and it can be observed that as remanent polarization increases, DIBL increases and as coercive field increases,

DIBL decreases. In particular, DIBL changed greatly in the region where the remanent polarization P_r was small and the coercive field E_c was large. Conversely, DIBL changed slightly in the region where the remanent polarization P_r was large and the coercive field E_c was small. As shown in Fig. 8, remanent polarization and coercive field must increase or decrease simultaneously to maintain a constant DIBL value. This indicates that the DIBL remains constant when the ratio of remanent polarization and coercive field, that is, P_r / E_c is constant. Therefore, the change of DIBL was obtained according to the ratio of remanent polarization P_r and coercive field E_c.

Under the device parameters in Fig. 9, the change of DIBL for P_r / E_c is shown as a parameter of ferroelectric thickness. As shown in Fig. 9, an increase in P_r / E_c corresponds to an increase in DIBL. This can be inferred from Fig. 8(b). In other words, as P_r / E_c increases in Fig. 8(b), the increasing rate of DIBL decreases and DIBL of GAA FET with ferroelectric eventually reaches that of GAA FET without ferroelectric due to the value in parentheses of Eq. (12). Particularly, when t_{fe} = 10 nm, the negative DIBL characteristics appear in the region of P_r / E_c < 8 pF/cm. As P_r / E_c is large, the change of DIBL according to the ferroelectric thickness decreases, and as P_r / E_c is small, the ferroelectric thickness has a large effect on the DIBL. It can also be observed that the DIBL becomes smaller than the case of t_{fe} = 0 nm regardless of the thickness of the ferroelectric due to the first term of Eq. (12).

The most ideal case is DIBL = 0 mV/V. In Fig. 9, it can be observed that as the ferroelectric thickness increases, the DIBL = 0 mV/V point appears only when P_r / E_c ≈8 pF/cm. A larger P_r / E_c implies a larger ferroelectric capacitance, and the SS increases at this time. Therefore, as P_r / E_c increases in the negative DIBL range, the absolute value of DIBL decreases, but the SS value increases, demonstrating a trade-off relationship between DIBL and SS [27-28].

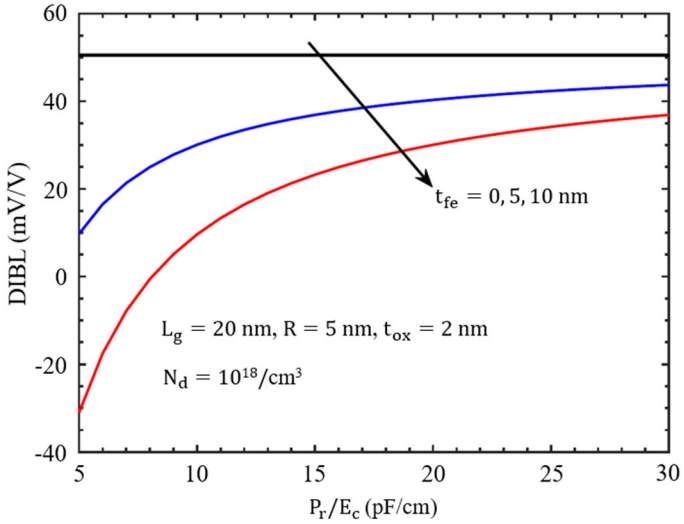
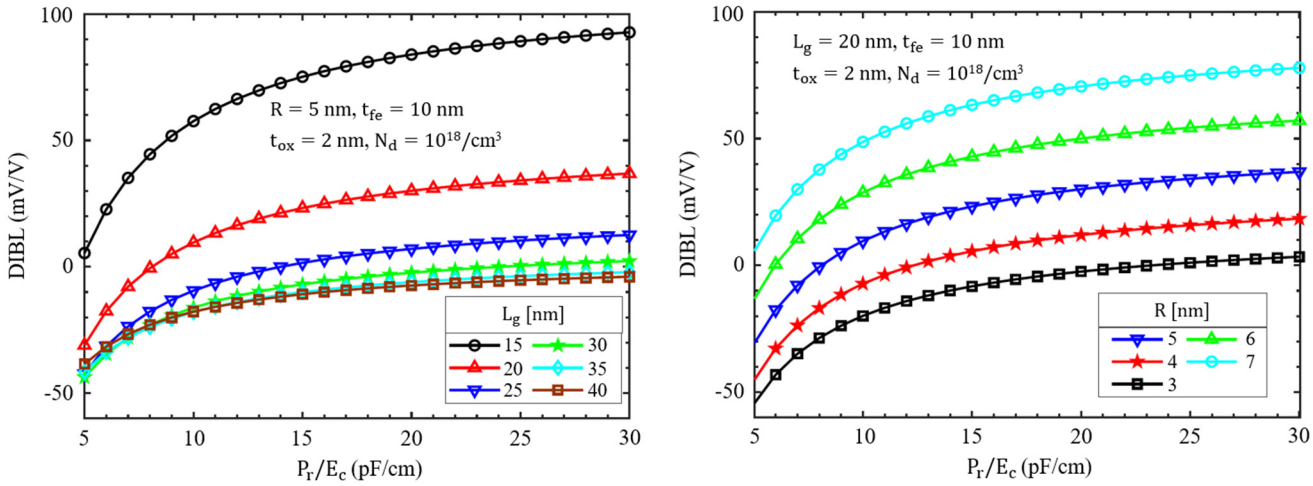


Fig. 9 DIBLs for P_r / E_c with the ferroelectric thickness as a parameter

The change of DIBL for P_r / E_c is shown in Figs. 10(a) and (b) with the channel length and channel radius as parameters. In Fig. 10(a), under the given device parameters, when the channel length is 25 nm or larger, and P_r / E_c is around 5 pF/cm, DIBL maintains almost constant. This is attributed to the fact that ΔQ becomes nearly constant when the channel length increases beyond 25 nm, as shown in Fig. 4(a).

In addition, as the channel length decreases to about 15 nm, the change of DIBL according to P_r / E_c increases, and as the channel length increases, the DIBL dependence on P_r / E_c decreases, and it is observed that there is little change in DIBL for P_r / E_c in L_g > 40 nm due to constant ΔQ. The P_r / E_c value at DIBL = 0 mV/V also increases as the channel length increases. In particular, the characteristics of DIBL < 0 mV/V can be observed in the entire range of P_r / E_c in the case of L_g > 30 nm under the given device parameters. This is because $-dV_{th1} / dV_{ds}$ becomes very small and is greatly influenced by the ferroelectric effects of the first term in Eq. (12).

Fig. 10(b) shows the case where the parameter is the channel radius, and DIBL increases as the channel radius increases. This is due to the relative decrease in channel length, ferroelectric thickness, and oxide thickness as observed in Figs. 7, 9, and 10(a) when R increases. Also, the change tendency of DIBL for P_r / E_c remains almost constant according to the channel radius regardless of the values of P_r / E_c. The P_r / E_c value of DIBL = 0 mV/V increases as R decreases.



(a) DIBLs for P_r / E_c with the channel length (b) DIBLs for P_r / E_c with the channel radius

Fig. 10 DIBLs for P_r / E_c with the channel length and radius as parameters

4. Conclusions

This study aims to investigate the relationship between the DIBL for the junctionless GAA FET with MFMIS structure using ferroelectric, and the P_r and E_c of the ferroelectric, as well as the device parameter. Therefore, an analytical DIBL model was presented, and it demonstrates good agreement with the DIBL values obtained from the relationship between drain current and gate voltage using 2D potential distribution.

Negative DIBL, or DIBR characteristics, became more pronounced as the ferroelectric thickness increased. This is attributed to the change in ferroelectric charge. In the DIBL contour for ferroelectric thickness and channel length, the area exhibiting negative DIBL characteristics did not demonstrate a uniform change, such as monotonic increase or monotonic decrease, but rather manifested a complex relationship. To satisfy a DIBL value of 0 mV/V, which is the most ideal characteristic, it is necessary to increase the ferroelectric thickness when channel radius and insulator thickness increase at a constant channel length. However, as the channel length increases, the ferroelectric thickness decreases significantly regardless of the channel radius and insulator thickness.

In the relationship between DIBL and the changes in P_r and E_c, which influences the characteristics of ferroelectric, it was observed that maintaining the P_r / E_c results in a constant DIBL value. The increase in ferroelectric thickness and channel radius, along with a decrease in channel length, leads to a larger DIBL change according to P_r / E_c. In addition, it was found that there is a trade-off relationship between DIBL and SS for the change of P_r / E_c in the range of negative DIBL. Therefore, the DIBL of junctionless GAA FET with ferroelectric could be considered using the analytical DIBL model presented in this paper.

Conflicts of Interest

The authors declare no conflict of interest.

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