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An Efficient Step-Up Converter with a Low Switch Stress

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Abstract

A novel approach is proposed for a high step-up and high efficiency converter with a low switch stress. The integrated boost-flyback converter uses coupled-inductor techniques to achieve high step-up voltage with low duty ratio, and thus the slope compensation circuit is disregarded. The proposed circuit topology improving high-gain ratio, increasing efficiency, reducing the secondary side of copper loss, and having an active-clamp effect that can reduce the switch stress on power components and have the energy feedback mechanism. Such a method of high efficiency and simple control can reduce cost which makes production size in increasing demand at present. Therefore, designing converters becomes a challenge when stepping up voltage with high efficiency and high power output. This thesis is a design of a high-efficiency step-up converter with low switch stress. The design is simple in that the circuit requires only a pulse width modulation (PWM) signal output. In addition, at cut-off time, the MOSFET generates a spike by way of a circuit sent to the output. This way can achieve the goal of energy recovery, an active-clamp, and can reduce the switch stress of power switch to improve circuit efficiency. Experimental results have confirmed that the proposed converter possesses high step-up, high efficiency, and low switch stress.

Keywords: step-up, low switch stress, active-clamp

1. Introduction

Alternative energy is currently most common in solar energy, wind power, and hydrogen fuel. The Grid-Tie or supply to high voltage equipment will be a challenge for PV systems, wind generators, and fuel cells to obtain high-voltage solar power that usually produces a number of solar cells in a series into a large-scale module. Moreover, to achieve high-voltage output, the number of solar cells in a series must also increase costs. For medium-sized wind power generators and fuel cell which output voltages are not high, wind power and fuel cells do not apply in a series. Regarding PV systems, wind turbines, and fuel cells as the power grid or supply to high voltage devices, using DC-to-DC power converters with high step-up is the most favorable choice. However, this high step-up converter from low voltage input to high voltage output easily leads to problems of inefficiency. Therefore, how to make good use of PV systems, wind turbines, and fuel cells to reduce costs and improve efficiencies is the primary focus of this study.

For example, K. C. Tseng [1, 2] of boost-flyback converters combined boost and flyback converters significantly improves the voltage gain ratio. Additionally, this structure has an active-clamp that can reduce the switch stress of power devices and energy regeneration mechanisms. This structure also has control of simple, high efficiency, and the secondary side

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of the stack that can improve voltage to gain characteristics. Rong-Jong Wai [3-6] enhanced the voltage gain ratio and reduced the switch stress of power devices based on coupled-inductor technology. Unfortunately, this structure has no boost-flyback converter secondary side of the stack effect to enhance the voltage gain. Spiazzi G. [7] of circuit structure is similar to the boost-flyback converter in that the circuit features added a forward converter. However, the circuit for forward and flyback types of output capacitors connected in a series to the load output causes the output voltage to ripple and the issue of greater for transformer air gap. Shih-Kuen Chang Chien [8] of circuit structure is similar to [7]. The circuits for forward and flyback type of output capacitors were connected similarly in a series to the load output, but the circuit structure enhanced the [7] voltage gain. Suman and Dwari [9] and Wuhua Li [10] of coupled inductor circuit used parallel arrays to improve the voltage gain, and a phase shift circuit in each group, which can obtain the average input current and reduce the loss of power components. The disadvantage is that control is not easy, and requires more pulse width modulation signals.

This article focuses on the design of a converter with high efficiency and high step-up. This circuit structure retains advantages and features of a boost-flyback converter, and increases the voltage gain ratio more effectively. Moreover, transformer copper loss can be reduced on the secondary side.

2. Design of Circuit

People gradually have the environmental awareness and start to use the renewable energy, such as solar power, wind power, and hydrogen fuel regarding green energy related circuit products and applications which output voltage is not high. Therefore, these need to use converters with high efficiency, high step-up, and high power. However, for high efficiency, high gain, and high power converters, the priority is to be designed with relatively high conversion efficiency. The priority has been compared with the 500-W efficiency in references [11] and [12]. However, the output power is larger and has a relatively large input current and loss of transformer and power components are enhanced. The trend of declining efficiency which in the design is more difficult to control. What way is necessary for using large heat sinks or cooling means to exclude losses arising from the heat, which easily create larger product size and weight. Although, the conversion efficiency can be improved by adapting the design, but now a number of high efficiency, high step-up and high power converter circuit design is very complicated, which is more control mode that caused by the difficulties of manufacture and its increased costs. To solve the demands of the conversion circuit that meet high-gain, high performance and design is not simple. For difficulties of design, large size, and poor efficiency, design costs are higher and yield many technical problems. This article combined with primary side and secondary side, improve high-gain ratio, increase its efficiency, reduce the secondary side of copper loss, and have having an active-clamp effect. Such a method which involves high efficiency and simple control can reduce the cost and size of the product.

2.1. Circuit Structure

This article describes the design of a high-efficiency step-up converter, which improves [1] can be seen from Fig. 1. This design has the advantage of low switch stress, high voltage gain, and high power. The proposed converter is shown in Fig. 2. The proposed step-up converter combined with primary-side and secondary-side. Primary-side having a boost circuit and secondary-side is used a voltage lift equivalent and flyback circuit to improve the voltage gain and reduce the secondary-side of the winding ratio and copper loss in the converter.

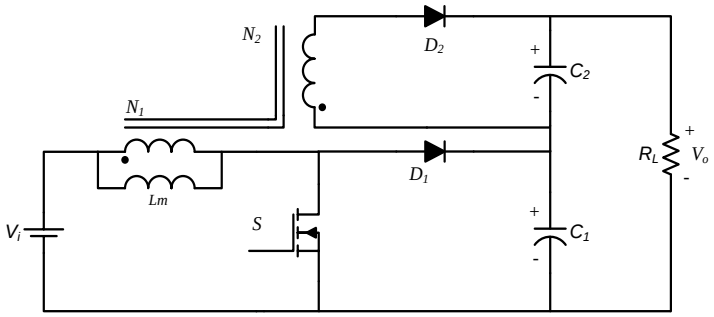


Fig. 1 Novel High-Efficiency Step-Up Converter

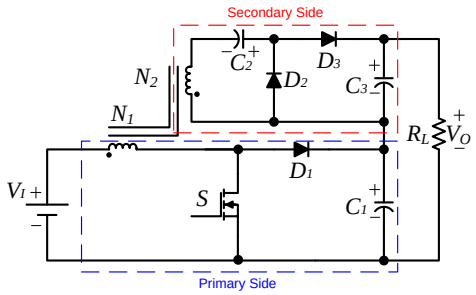


Fig. 2 Circuit configuration of the proposed step-up converter

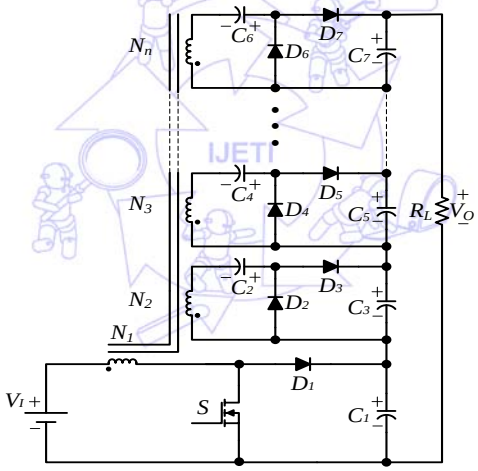


Fig. 3 Proposed step-up converter with the secondary-side of the series

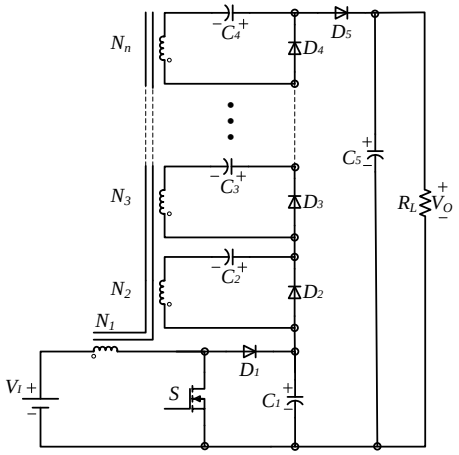


Fig. 4 Proposed step-up converter with the secondary side of the simplified component series

2.2. Working Principle

Fig. 5 shows the characteristic waveforms during five operation modes of the proposed converter in one switching period. The circuit operation mode status is shown in Fig. 6. The operating principle of continuous-conduction mode for proposed converter is presented in detail.

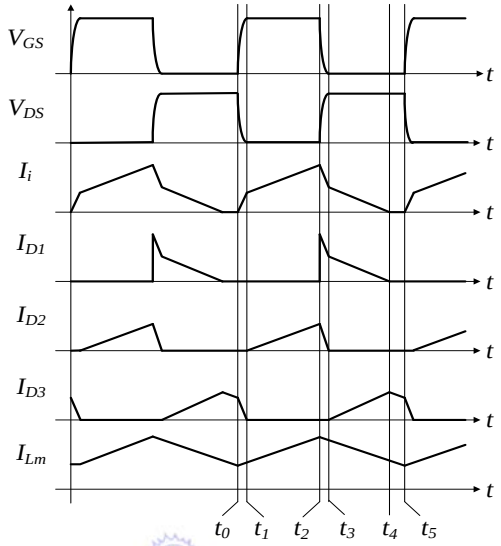


Fig. 5 Characteristic waveforms of the proposed converter under CCM operation during one switching period

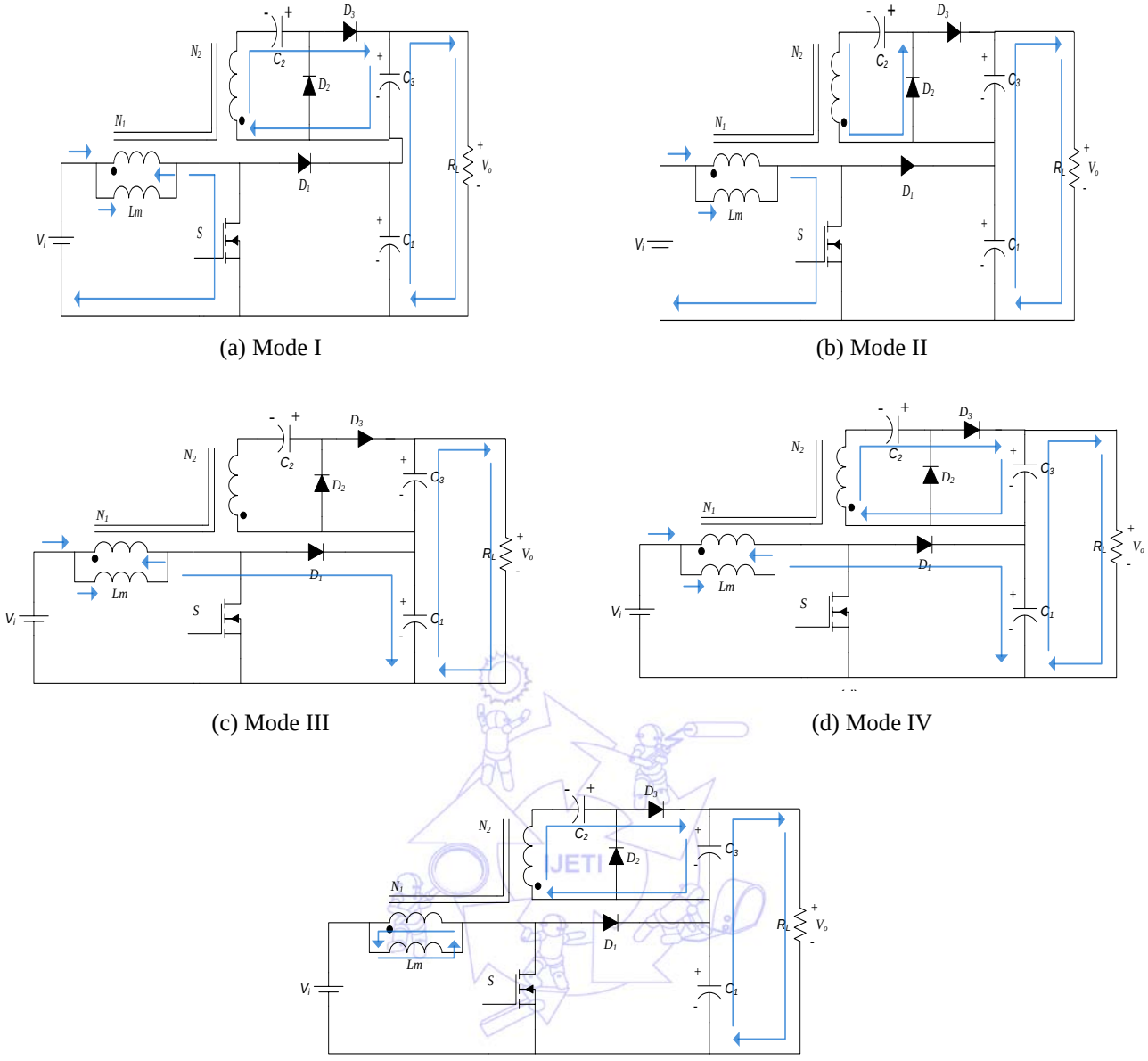
Mode I [t_0, t_1]: At $t = t_0$, switch S is turned on. Diode D_1 and D_2 are turned off and D_3 is turned on. The voltage equation of the primary-side of coupled inductor is $V_i = V_{Lm} + V_{Lk1}$. Simultaneously, the voltage V_{N2} is induced. Therefore, the primary-side current of the coupled inductor i_{Lk1} increases linearly and the secondary current is decreases linearly. When current i_{N2} becomes zero, diode D_3 is turned off. The magnetizing inductor L_m starts to charge by the DC source V_i and the diode D_2 starts to turned on. As current i_{Lk1} is equal to $i_{Lm} + n_2 \cdot i_{N2}$ at $t = t_1$, this operating mode is ended.

Mode II [t_1, t_2]: During this time interval, switch S is turned on. Diodes D_1 and D_3 are turned off, and D_2 is turned on. The magnetizing inductor L_m is charged by the DC-source V_i. Meanwhile, on the secondary-side winding N_2 of the voltage V_{N2} is charge to the capacitor C_2. Voltage V_{C2} is approximately equal to $nV_{N2.}$ When current i_{Lk} becomes zero, diode D_1 is turned on. This operating mode is ended at $t = t_2$.

Mode III [t_2, t_3]: During this time interval, switch S is turned off. Diodes D_1 and D_2 are turned on and D_3 is turned off. The energy of the leakage inductance L_{k1} and magnetizing inductor L_m charge to the parasitic capacitor C_{ds} of switch S. Capacitor C_2 is charged by V_{N2}. While the capacitor voltage V_{ds} is equal to $V_i + V_{Lk1}$ at $t = t_3$, diode D_1 conducts and this operating mode is ended.

Mode IV [t_3, t_4]: At $t = t_3$, switch S is turned off. Diodes D_1 and D_3 are turned on, D_2 is turned off. The energy of DC-source V_i, the leakage inductance L_{k1} and magnetizing inductor L_m are charge to capacitor C_1. The energy of leakage inductance L_{k1} is recycled. The current i_{Lk1} decreases quickly. According to the leakage inductance L_{k1}, the secondary-side current i_{D3} is decreased. At $t = t_4$, the primary-side current i_{D1} is equal to zero, diode D_1 is cut off. This operating mode is ended.

Mode V [t_4, t_5]: During this time interval, switch S is still turned off. Diodes D_1 and D_2 are turned off, diode D_3 is turned on. The voltage of the secondary-side V_{N2} and V_{C2} are still released energies to the capacitor C_3. This mode is ended at $t = t_5$ during S is turned on at the beginning of the next switching period.



(a) Mode I

(b) Mode II

(c) Mode III

(d) Mode IV

(e) Mode V

Fig. 6 Current flow path of the operation modes at CCM

2.3. Steady-State Analysis

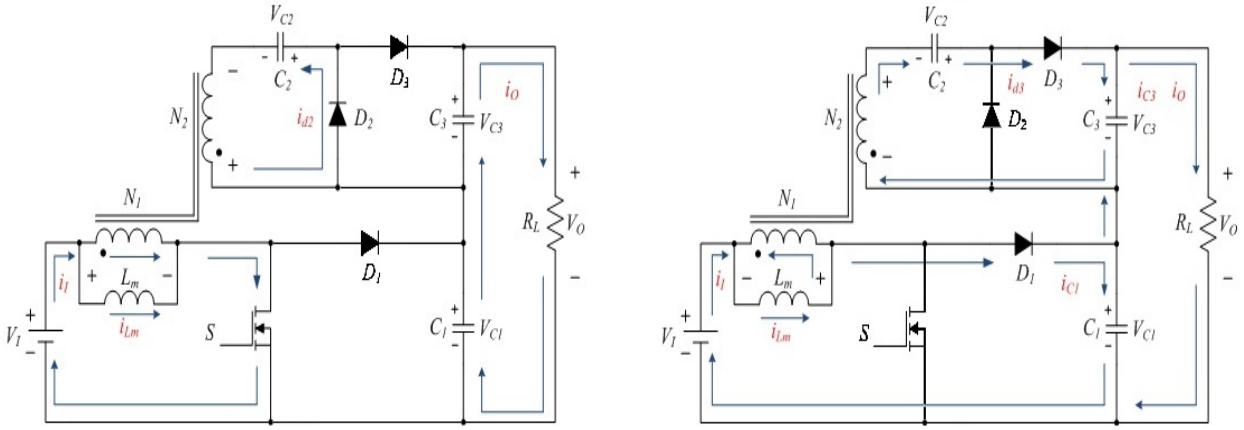
To analyze the steady-state characteristics of the proposed converter under CCM operation, the leakage inductance, winding resistance and the transient characteristics of the MOSFET are neglected. The coupled inductor is modeled as a magnetizing inductor L_m, and assuming ideal power devices and that capacitors C_1, C_2 and C_3 are sufficiently large and output voltage are considered to be constant.

During the equivalent circuit of switch S turned on and the equivalent circuit is shown in Fig. 7(a). The voltage across magnetizing inductance V_{Lm} can be denoted $V_i = V_{Lm}$. Current $\Delta i_{Lm(on)}$ is represented as

$$\Delta i_{Lm(on)} = \frac{V_i}{L_m} \cdot D \cdot T_S, \ \left(0 \le t \le DT_S\right) \tag{1}$$

The voltage-lift capacitor V_{C2} can be written as

$$V_{C2} = V_{N2} = V_i \cdot \frac{N_2}{N_1} \tag{2}$$



(a)Switch *S* turned on (b) Switch *S* turned off

Fig. 7 The equivalent circuit of the proposed *converter* at CCM operation

During the equivalent circuit of switch *S* turn off, the diodes *D1* and *D3* are conducted and the equivalent circuit is shown in Fig. 7(b). The voltage across magnetizing inductance V_{Lm} can be denote

$$V_{Lm} = V_{C1} - V_i \tag{3}$$

Current $\Delta i_{Lm(off)}$ is expressed as

$$\Delta i_{Lm(off)} = \frac{V_{C1} - V_i}{L_m} \cdot (1-D) \cdot T_s, \ \left(DT_S \le t \le T_S\right) \tag{4}$$

and

$$V_{N2} = \left(V_{C1} - V_i\right) \cdot \frac{N_2}{N_1} \tag{5}$$

$$V_{C3} = V_{N2} + V_{C2} \tag{6}$$

Based on the volt-second balance principle, the voltage of coupled inductor V_{Lm} can be expressed as follows:

$$\Delta i_{Lm}^{+} = \Delta i_{Lm}^{-} \tag{7}$$

Substituting (1) and (4) into (7), the voltage across the capacitor *C1* can be derived as

$$V_{C1} = \frac{1}{1-D} V_i \tag{8}$$

and

$$V_O = V_{C1} + V_{C3} \tag{9}$$

Substituting (2), (6) and (8) into (9), the output voltage V_o can be derived as

$$\frac{V_o}{V_I} = \frac{1 + \frac{N_2}{N_1}}{1-D} \tag{10}$$

The circuit of the voltage gain versus the duty ratio under various turn ratios of the coupled inductor is shown in Fig. 8.

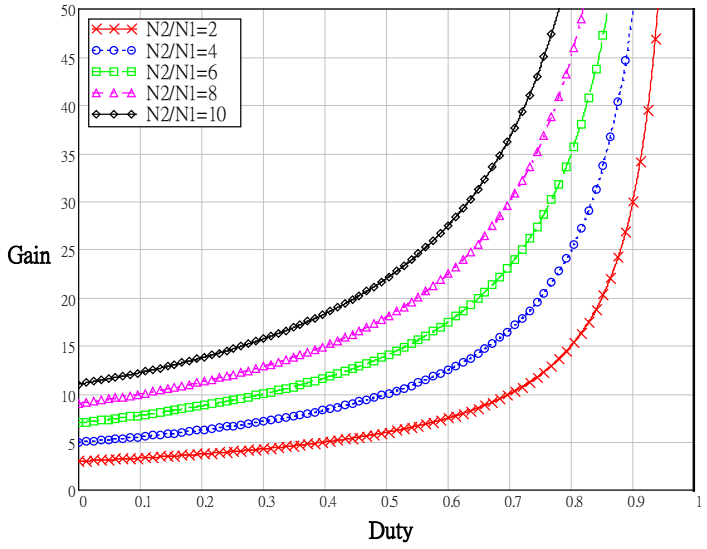


Fig. 8 Voltage gain and duty ratio of the proposed converter under different turn ratios

2.4. Effects of the ESRs of the Semiconductor Devices

Fig. 9 shows the equivalent circuit including inductor copper inductances r_{L1} and r_{L2}, on resistances of diode r_{D1}, r_{D2} and r_{D3}, and on resistance $r_{DS(on)}$ of the main switch. The following conditions of the proposed converter are assumed in this analysis of the Model.

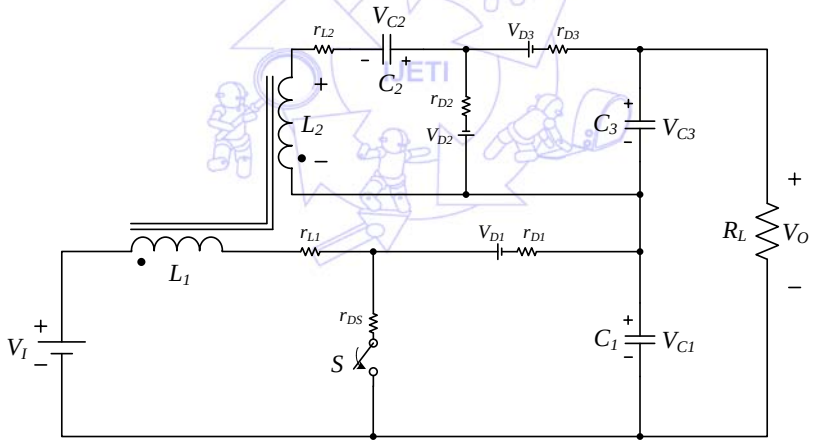


Fig. 9 Equivalent circuit with copper and semiconductor losses

(1) The main switch parasitic capacitor and the diode capacitor are excluded.

(2) During the switch is turned on can be modeled a resistance $r_{DS(on)}$, and during the switch turned off can be modeled an infinite resistance.

(3) The diodes are modeled by the forward voltage V_{D1}, V_{D2} and V_{D3}, and the forward resistances r_{D1}, r_{D2} and r_{D3}. When the diodes are reversed-biased, they can be modeled by an infinite resistance.

(4) The effects of leakage inductances L_{k1} and L_{k2} are neglected.

(5) Switching loss and ESRs of capacitors are neglected.

(6) Assumed the magnetizing inductor is sufficiently large to ensure a small-ripple current approximation.

(7) To consider DC components during the off period, the average current is $i_{L1} = i_{L1}(t)$, and the average current is $i_{L2} = i_{L2}(t)$.

(8) The capacitors C_1, C_2 and C_3 are assumed to be large enough and output voltage V_o is constant.

Based on the Kirchhoff's voltage law (KVL) principle, during the switch S is turned on as shown in Fig. 10(a), the following equations can be represented as follow

$$V_i = V_{L1(on)} + i_{L1} \cdot r_{L1} + i_{DS} \cdot r_{DS} \tag{11}$$

$$V_{L1(on)} = V_i - i_{L1}\left(r_{L1} + r_{DS}\right) \tag{12}$$

$$V_{C2} = \frac{N_2}{N_1} V_{L1(on)} - i_{D2}\left(r_{L2} + r_{D2}\right) - V_{D2} \tag{13}$$

The current of capacitors C_1, C_2 and C_3 are given as follows:

$$i_{C1(on)} = -\frac{V_o}{R_L} = -i_o \tag{14}$$

$$i_{C2(on)} = i_{D2} \tag{15}$$

$$i_{C3(on)} = -\frac{V_O}{R_L} = -i_O \tag{16}$$

During the main switch S is turned off as shown in Fig. 10(b), the following equations can be represented as follow

$$V_{C1} = V_i + V_{L1(off)} - i_{L1}\left(r_{L1} + r_{D1}\right) - V_{D1} \tag{17}$$

$$V_{C3} = \frac{N_2}{N_1} V_i + V_{C2} - i_{L2}\left(r_{L2} + r_{D3}\right) - V_{D3} \tag{18}$$

$$V_o = V_{C1} + V_{C3} = V_i + \left(1 + \frac{N_2}{N_1}\right) V_{L1(off)} + V_{C2} - i_{L1}\left(r_{L1} + r_{D1}\right) - i_{L2}\left(r_{L2} + r_{D3}\right) - V_{D1} - V_{D3} \tag{19}$$

The current of C_1, C_2 and C_3 are givens as follow

$$i_{C1(off)} = i_{L1} - \frac{V_o}{R_L} \tag{20}$$

$$i_{C2(off)} = -i_{L2} \tag{21}$$

$$i_{C3(off)} = i_{L2} - \frac{V_o}{R_L} \tag{22}$$

Substituting (13) into (19), the inductor voltage $V_{L1(off)}$ is derived as

$$V_{L1(off)} = \frac{1}{1+n}\cdot[V_O - V_i(1+n) + n\cdot i_{L1}(r_{L1}+r_{DS}) + i_{D2}(r_{L2}+r_{D2}) + i_{L1}(r_{L1}+r_{D1}) + i_{L2}(r_{L2}+r_{D3}) + (V_{D1}+V_{D2}+V_{D3})] \quad (23)$$

Based on the amp-second balance principle, from (14), (15), (16) and (20), (21), (22) can be rewritten as follows:

$$\int_0^{DT_S} i_{C1(on)}dt + \int_{DT_S}^{T_S} i_{C1(off)}dt = 0 \quad (24)$$

$$\int_0^{DT_S} i_{C2(on)}dt + \int_{DT_S}^{T_S} i_{C2(off)}dt = 0 \quad (25)$$

$$\int_0^{DT_S} i_{C3(on)}dt + \int_{DT_S}^{T_S} i_{C3(off)}dt = 0 \quad (26)$$

According to (26), the current flow path the C_3 can be presented as

$$-\frac{V_O}{R_L}\cdot DT_S + \left(i_{L2} - \frac{V_O}{R_L}\right)\cdot(1-D)T_S = 0 \quad (27)$$

Form equation (27), the current i_{L2} is determined as

$$i_{L2} = \frac{1}{1-D}\cdot\frac{V_O}{R_L} \quad (28)$$

According to (24), the current flow path on the C_1 can be presented as

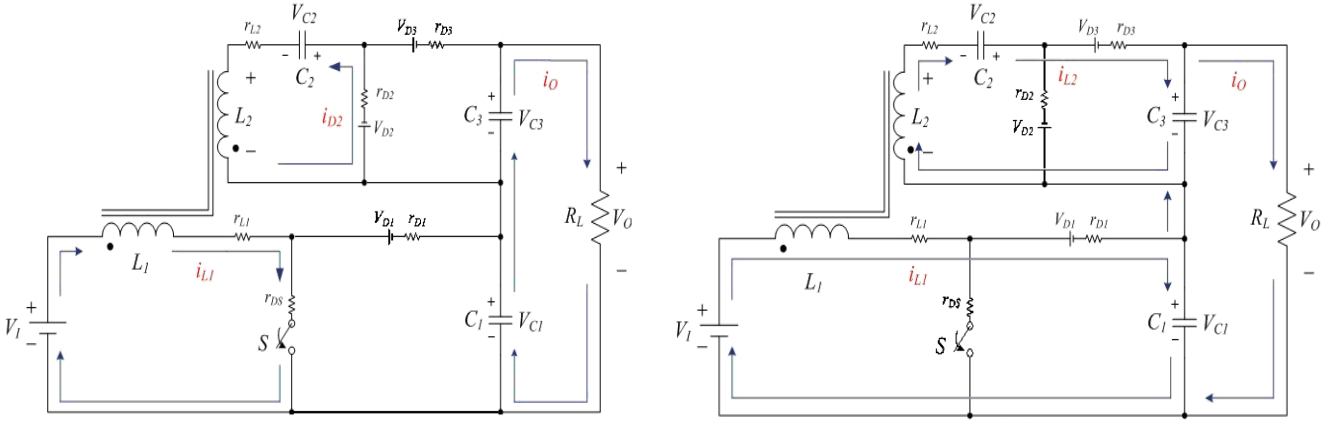
$$-\frac{1}{1-D}\cdot\frac{V_O}{R_L}\cdot DT_S + i_{C1}\cdot(1-D)T_S = 0 \quad (29)$$

Form equation (29), the current i_{L1} is determined as

$$i_{L1} = \frac{1}{1-D}\cdot\frac{V_O}{R_L} \quad (30)$$

Substituting (28) into (25), the current flow path i_{D2} can be derived as follows

$$i_{D2} = i_{L2}\frac{D}{1-D} \quad (31)$$



(a) Switch turned on (b) Switch turned off

Fig. 10 Equivalent circuit

Where in the steady state, the principle of volt-second balance can be given as equation:

$$\begin{aligned}\left[V_i - i_{L1}(r_{L1}+r_{DS})\right]\cdot DT_S = \frac{1}{1+n}\cdot\big[&V_O - V_i(1+n) + n\cdot i_{L1}(2r_{L1}+r_{DS}) \\ &+ i_{D2}(r_{L2}+r_{D2}) + i_{L1}(r_{L1}+r_{D1}) \\ &+ i_{L2}(r_{L2}+r_{D3}) + (V_{D1}+V_{D2}+V_{D3})\big]\cdot(1-D)T_S\end{aligned} \tag{32}$$

Where $n = \frac{N_2}{N_1}$

From equation (34), the equation can be rewritten as

$$\begin{aligned}V_O = \left(\frac{1+n}{1-D}\right)V_i - \Big\{&\frac{1+n}{1-D}\left[i_{L1}\cdot D(r_{L1}+r_{DS})\right] + i_{L1}\cdot n(r_{L1}+r_{DS}) \\ &+ i_{D2}(r_{L2}+r_{D2}) + i_{L1}(r_{L1}+r_{D1}) \\ &+ i_{L2}(r_{L2}+r_{D3}) + (V_{D1}+V_{D2}+V_{D3})\Big\}\end{aligned} \tag{33}$$

Substituting (28), (30) and (31) into (33), the equation can be rewritten as

$$\begin{aligned}V_O = \left(\frac{1+n}{1-D}\right)V_i - \Big\{&\frac{(1+n)D}{1-D}\cdot i_{L1}(r_{L1}+r_{DS}) + n\cdot i_{L1}(r_{L1}+r_{DS}) + \frac{D}{1-D}\cdot i_{L1}(r_{L2}+r_{D2}) \\ &+ i_{L1}(r_{L1}+r_{D1}+r_{L2}+r_{D3}) + (V_{D1}+V_{D2}+V_{D3})\Big\}\end{aligned} \tag{34}$$

From equation (34), the voltage conversion ratio V_O/V_i is represented as follows

$$\frac{V_O}{V_i} = \frac{\left(\frac{1+n}{1-D}\right)\cdot\left(1-\frac{1}{\frac{1+n}{1-D}}\cdot\frac{(V_{D1}+V_{D2}+V_{D3})}{V_i}\right)}{1+\left[\frac{r_{L1}(1+n)+r_{L1}+r_{DS}(1+n)+r_{D1}}{(1-D)^2\cdot R_L} + \frac{r_{L1}(1+n)+n\cdot r_{DS}+r_{L2}+r_{D1}+r_{D3}}{(1-D)\cdot R_L}\right]} \tag{35}$$

Where $n = \frac{N_2}{N_1}$

The voltage gain and efficiency affected by different ESRs with coupled inductor is shown in Fig. 11 and Fig. 12. The maximal voltage gain is constrained by the equivalent series resistances, and the efficiency will be decreased by the extreme duty ratio.

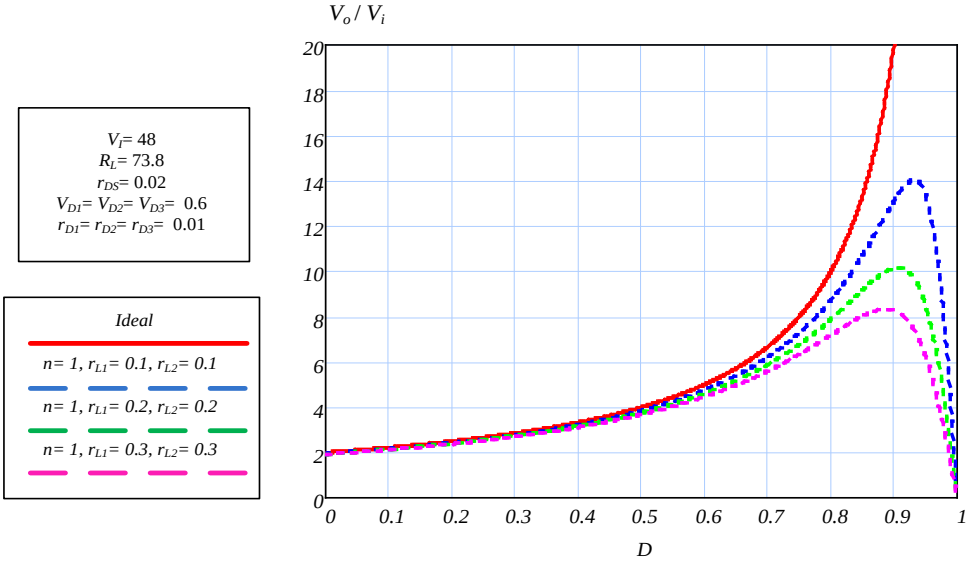


Fig. 11 Voltage gain versus duty ratios under different ESRs with coupled inductor

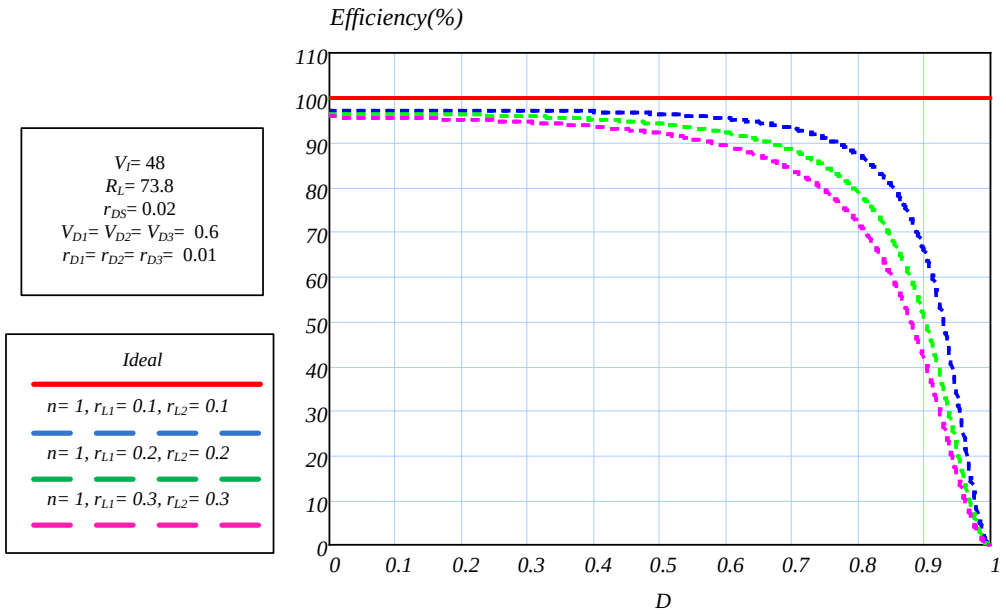


Fig. 12 Efficiency versus duty ratios under different ESRs with coupled inductor

Neglecting the equivalent series resistance of the proposed converter, the ideal voltage gain can be expressed as

$$M_{CCM} = \frac{V_O}{V_i} = \frac{1+\frac{N_2}{N_1}}{1-D} \tag{36}$$

According to (55), the equation can be reorganized and the equivalent circuit is shown in Fig. 13 as follows

$$V_i(1+n) = V_O(1-D) + i_{L1}\left[r_{L1}(1+n) + r_{DS}(1+n) + r_{L2} + r_{DX}(1-D)\right] + V_{DX}(1-D) \tag{37}$$

Where $r_{DX} = r_{D1} + r_{D2}\frac{D}{1-D} + r_{D3}$

$V_{DX} = V_{D1} + V_{D2} + V_{D3}$

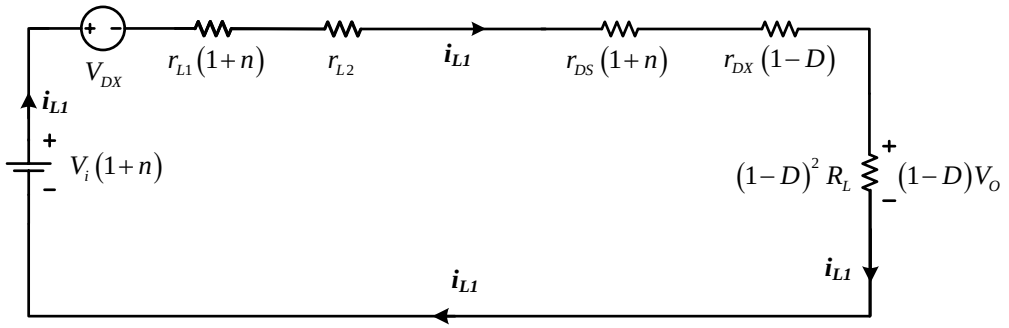


Fig. 13 Equivalent circuit corresponding to Eq. 37

The input power and output power of the converter can be calculated as shown in equation (38) and (39), respectively.

$$P_{in} = \left(1+\frac{N_2}{N_1}\right)V_i \cdot i_{L1} \tag{38}$$

$$P_{out} = (1-D)V_O \cdot i_{L1} \tag{39}$$

$$\eta = \frac{P_{out}}{P_{in}} \tag{40}$$

According to the equation (38), (39) and (40), the converter efficiency can be derived as follows

$$\eta = \frac{1-\left(\frac{1+n}{1-D}\right)\cdot\frac{\left(V_{D1}+V_{D2}+V_{D3}\right)}{V_i}}{1+\left[\frac{r_{L1}\left(1+n\right)+r_{L1}+r_{DS}\left(1+n\right)+r_{D1}}{\left(1-D\right)^2\cdot R_L}+\frac{r_{L1}\left(1+n\right)+n\cdot r_{DS}+r_{L2}+r_{D1}+r_{D3}}{\left(1-D\right)\cdot R_L}\right]} \tag{41}$$

Where $n = \frac{N_2}{N_1}$

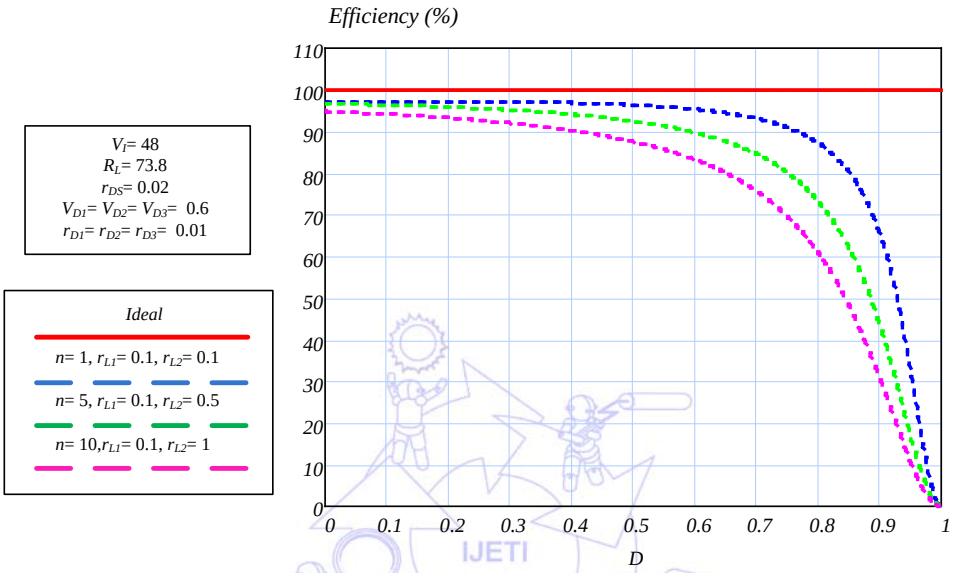


Fig. 14 The efficiency versus duty ratio under various turn ratios and ESRs

From equation (41) shows that the efficiency is affected by the equivalent series resistance. Fig. 14 shows the efficiency affected by various turns ratios and ESRs.

2.5. Comparison of Converter Voltage Gain

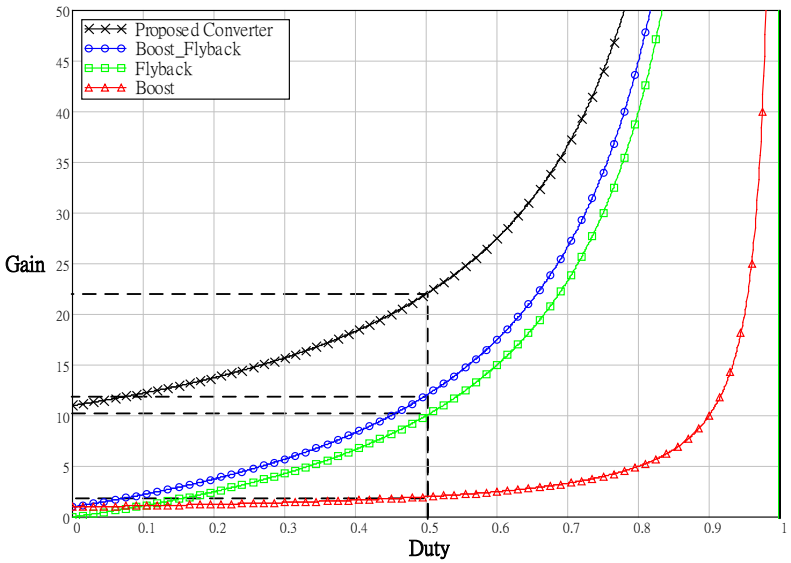


Fig. 15 Comparison of converter voltage gain

Fig. 15 shows a comparison of the converter voltage gain and the set $N_2 / N_1 = 10$. When working in a 50 % duty cycle, the boost converter voltage gain is the lowest. Second, the setting of the winding ratio is $N_2 / N_1 = 10$; therefore, the flyback converter voltage gain is greater than the boost converter. The boost-flyback converter is a combination of the boost converter and flyback converter. The structure has many advantages; however, the voltage gain is only slightly larger than that of the flyback converter. The proposed step-up converter is improved with the boost-flyback converter, which has features and benefits of the boost-flyback converter. Furthermore, the proposed converter has a much higher efficiency in voltage gain than the other converters.

3. Simulation and Experimental Results of the Proposed Converter

3.1. Simulation for The Proposed Converter

Software of SIMPLIS was used to simulate the proposed step-up converter in this study. The parameters of the circuit design are shown in Table 1.

Table 1 Design parameters of prototype

Item	Parameter
Input voltage range	70 V_{DC} ~ 100 V_{DC}
Input current range	17 ~ 25 A
Output voltage	335 V_{DC}
Output current	5 A
Output power	1600 W

Fig. 16(a) shows the simulation waveform of 400W, which is able to tell that I_{Lm} lowest current has been greater than zero. This means that the work patterns have full access to the continuous conduction mode. In addition, the circuit V_{DS} voltage waveform is perfect in that and no spike is generated. The 1600W simulation waveform is shown in Fig. 16(b). The waveform has not changed much since the operation at 400W into the continuous conduction mode afterward. Only the current peaks gradually increased.

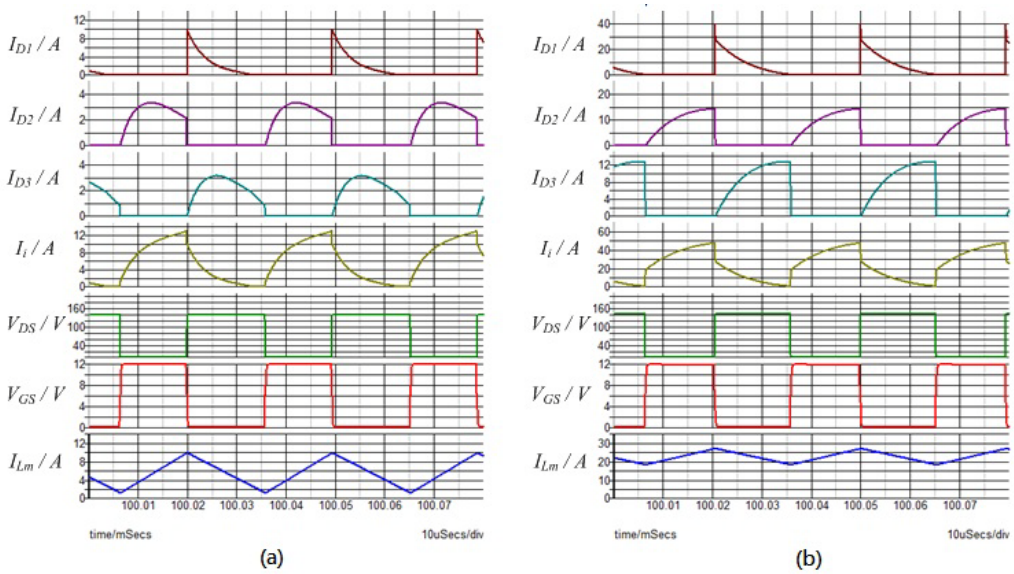


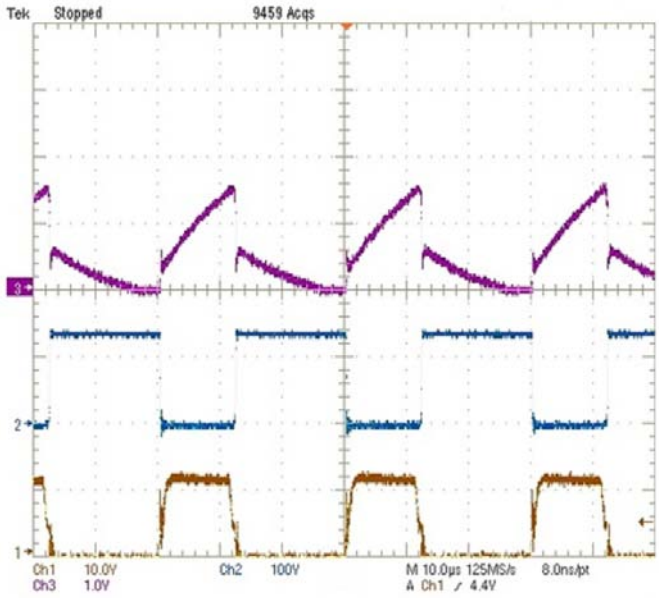
Fig. 16 Simulation waveform (a) 400 W, (b) 1600 W

3.2. Experimental Results for The Proposed Converter

Each component of the circuit is used in design that will affect efficiency. The experimental circuit parameters are shown in Table 2.

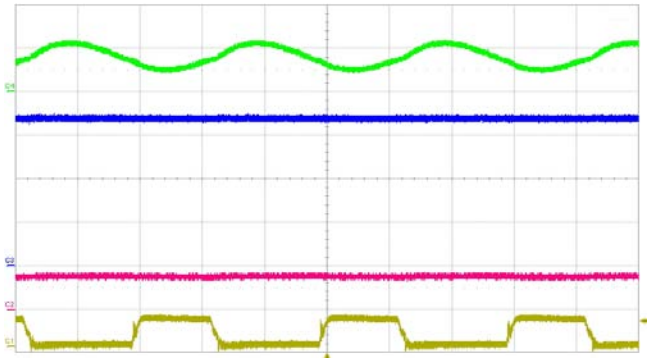
Table 2 Utilized components of prototype

Item	Parameter
MOSFET *S*	FQA65N20
Diode D_1	V60200PG
Diode D_2 / D_3	20CTH03FP
Magnetize inductance (L_m)	115*u*H
Leakage inductance	0.93*u*H
N_1 ：N_2	38 : 55
PWM Control IC	UC3845
Operating frequency	33*k* Hz



ch1:V_{GS}(10V/Div), ch2:V_{DS}(100V/Div), ch3:I_i (10A/Div)　　ch1：V_{GS} (10V/Div), ch2: V_{DS} (100V/Div), ch3: I_i (20A/Div)

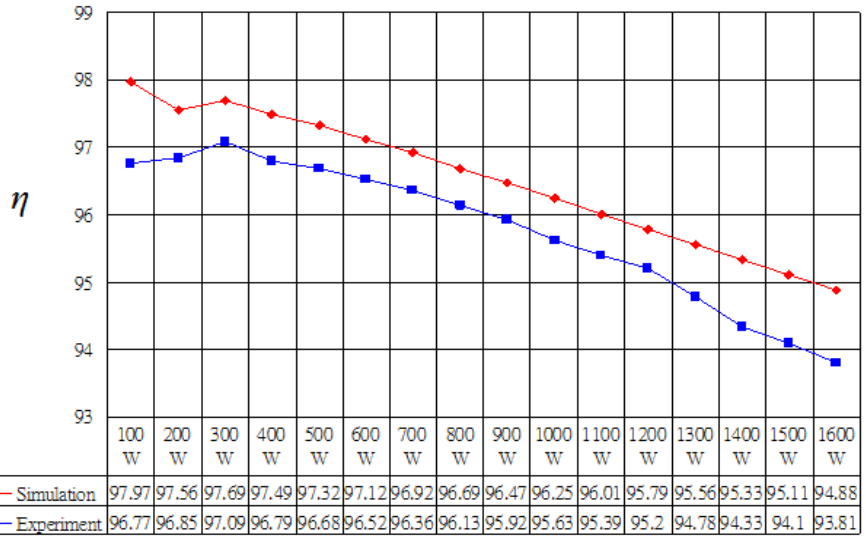
Fig. 17 Waveform measurement of proposed topology: (a) 400W, (b) 1600W



ch1:V_{GS}(20V/Div), ch2:V_I(100V/Div),ch3:V_O(100V/Div), ch4:I_O(5A/Div)

Fig. 18 Input and output voltage, and output current waveform

The waveform measurement of the proposed STEP-up Converter is shown in Fig. 17. The circuit can be measured by the waveform diagram similarly to the simulation results. The input and output voltage, and output current waveform are shown in Fig. 18.



	100 W	200 W	300 W	400 W	500 W	600 W	700 W	800 W	900 W	1000 W	1100 W	1200 W	1300 W	1400 W	1500 W	1600 W
Simulation	97.97	97.56	97.69	97.49	97.32	97.12	96.92	96.69	96.47	96.25	96.01	95.79	95.56	95.33	95.11	94.88
Experiment	96.77	96.85	97.09	96.79	96.68	96.52	96.36	96.13	95.92	95.63	95.39	95.2	94.78	94.33	94.1	93.81

Fig. 19 Comparison of simulation and implementation efficiency

For experimental waveform measurement, the input supply voltage source involved seven 12V lead-acid batteries. The output was a resistive load box, and the circuit efficiency of the simulation and experiment are shown in Fig. 19, which demonstrated the highest efficiency of 97.09 % at 300W. Moreover, when at full load, 1600W demonstrated 93.81 % efficiency performance. In addition, Fig.13 illustrates the efficiency that gradually decreased operate at 500W after. The main reason is that when the power device conduction. The flow through power devices and the transformer input current resulting loss has increased significantly ($P_{Loss}=I^2R$), which is a feature of the high power and high step-up converter. The duty cycle can be raised to resolve this problem of decreasing efficiency, and the current peaks can be smooth in a cycle. This is a feature of the past involving the duty cycle being too high and resulting in decreased efficiency. After the increased duty cycle, the resulting loss that parasitic elements is much smaller than the input current in the power components [14].

4. Conclusion

These voltages are low for photovoltaic systems, fuel cells, wind generators and uninterruptible power systems, whose voltages are not high; therefore, they require high-gain and high-power converters to raise voltage supply devices such as power grids and electric vehicles. Many high-power converters currently have control of complex and costly problems. The proposed circuit topology improving high-gain ratio, increasing efficiency, reducing the secondary side of copper loss, and having an active-clamp effect that can reduce the switch stress on power components and have the energy feedback mechanism. Such a method of high efficiency and simple control can reduce cost and product size. The circuit configuration of the proposed converter topology demonstrated the highest efficiency of 97.09 % at 300W in the experiment. Moreover, when at full load, 1600W demonstrated 93.81 % efficiency performance.

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