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Hardware Implementation of Road Network Extraction Using Simplified Gabor Wavelet in Field Programmable Gate Array

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Abstract

Automatic detection of road networks from the satellite and aerial images is the most demanded research area, and it is used for various remote sensing applications. The Simplified Gabor Wavelet based approaches are used to extract the road network automatically. In this paper, a field programmable gate array architecture designed for automatic extraction of road network using Simplified Gabor Wavelet is proposed. The hardware implementation results are compared with software implementation results. The performance measures such as completeness, correctness and quality are calculated. In the software implementation, the average value of completeness, correctness, and quality of various images are 91%, 98%, and 89% respectively. In the hardware implementation, the average value of completeness, correctness, and quality are 89%, 97%, and 87% respectively. The performance of the proposed algorithm is also proved in noisy images. These measures prove that the proposed work yields road network very resembling to reference road map.

Keywords: road network extraction, simplified Gabor wavelet, field programmable gate array, connected component

1. Introduction

Automatic detection of road networks from the satellite and aerial images is the most demanded research subject and it is used in many computer vision applications [1]. The updating of road network databases is essential to many GIS (Geographic Information System) applications like navigation, urban planning, route planning, health care accessibility planning, land cover classification and infrastructure management etc. The proposed work is boundary and centerline of road network extraction using Simplified Gabor Wavelet (SGW) and FPGA architecture is proposed for this road network extraction method.

The remaining part of this paper is organized as follows. In Section 2, a literature survey on road network extraction is given. Section 3 presents road network extraction using SGW. Section 4 provides the results and discussion of the proposed algorithm. In Section 5, FPGA Architecture for Road Network Extraction using SGW is proposed. Section 6 gives FPGA implementation and synthesis results of the proposed architecture, and Section 7 provides the conclusion of the paper.

2. Literature Survey

Many research works have been proposed for automatic road network extraction using wavelet transform for the past few years. Guan et al. have presented an approach for road centerlines extraction and width estimation [1]. Canny is used to detecting

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the edge of a line, and two parallel lines are extracted from the edges through progressive probabilistic Hough transform. A wavelet transform based road centerline extraction method has been proposed by Chen [2]. Images are preprocessed using thresholding method and 2D wavelet transform is applied to identify the road regions and the thinning algorithm is used to detect the centerline of the road. Zhu et al. have proposed the road network recognition approach using morphological characteristics [3]. It is based on morphological operations and a line segment match method. The accuracy of the proposed approach is proved with the help of quantitative measures.

Automatic road network extraction using wavelet transform has been presented by Tuncer [4]. Karhounen-Louve Transform (KLT) based wavelet filter banks are used for preprocessing and then, the fuzzy algorithm is used to detect the road. Parthasarathi and Pushpamitra implemented an automatic road extraction for high-resolution satellite images using FPGA [5]. The road is extracted by using level set and mean shift method and implemented on Xilinx Spartan3 FPGA device. Road extraction using Stationary wavelet transform has been presented by Udomhunsakul [6]. The Stationary wavelet transform is applied to the images and the products of Wavelet coefficients at different scales are calculated to locate and identify road pixels.

Hao et al. [7] presented Gabor Wavelet (GW) based edge feature extraction through a reasonable choice of directions and scales. Jiang et al. [8] proposed a Simplified Gabor Wavelet (SGW) based image edge detection. This algorithm has achieved a performance level in terms of detection accuracy similar to that based on GW, but it requires the smaller amount of computation. Hu et al. [9] have presented a method for automatic road extraction which includes three steps, road seed pixel is identified, road tracking and growing road segment. A road tree is constructed to identify the road network. Jin and Davis [10] integrated two detectors to detect road centrelines. The outputs of fine scale image segmentation based detector and fuzzy based multiscale curvilinear detector are combined together to get road network and path searching algorithm is used for this integration. Shi et al.[11] have presented road extraction method for an urban area. It includes two stages, image classified as road class and nonroad class using path openings and closings and road class are refined by shape features. A support vector machine based road centerline has been presented by Huang & Zhang [12]. This method uses both geometrical features of road and spectral variation and hybrid of geometrical and spectral information are analyzed using Support Vector Machine (SVM) classifier. The algorithm is implemented on multispectral images and the results are given.

Maurya et al. [13] have presented a method for road extraction using morphological and K-mean clustering. Road regions are separated from high-resolution image using K-means clustering. The results are proved with the help of the quality measures. Mena & Malpica [14] have proposed an approach for automatic road extraction in rural and semi-urban areas which include four modules, data preprocessing, binary segmentation based on texture progressive analysis, binary image is vectorized by means of skeletal extraction and morphological operations, and the algorithm is evaluated by comparing with manually drawn road map.

Singh and Garg [15] have proposed a road network segmentation technique using morphological operations. Road regions are segmented using average intensity values and morphological operators are used for further processing. Miao et al. [16] have proposed a method for road centerline extraction from classified image which consists of the three stages, extraction of feature points using tensor voting, kernel density estimation is used to find probability of each pixel being located on the road centerline and centerline of road is formed by linking the projected feature using geodesic method. Wavelet transforms play a very vital role in road network extraction from the satellite image. Simplified Gabor Wavelet transform is very optimum for feature segmentation and that is proposed for edge detection. In this work, SGW is proposed for road network segmentation. For real-time implementation, image processing applications must meet the hardware requirement. Hence, FPGA implementation of road network extraction using SGW is proposed. Both boundary and centerline of the road network are extracted using SGW and its hardware implementation is proposed in this work.

3. Methodology of Road Network Extraction Using SGW

This proposed work for automatic road centerline extraction method from high-resolution satellite image is based on SGW and morphological operators. The methodology includes adaptive global thresholding method, connected component approach, road boundary extraction using SGW, and morphological thinning. The satellite image is converted into the gray image. Adaptive global thresholding is applied to segment approximated road region from the image. The histogram of the satellite image is analyzed and divided into four main sections to obtain the desired threshold value for segmentation. From this technique, approximated road regions are identified. The pixels which lie in that region are assigned to the value 1 and remaining all the pixels are made to 0. Now, gray image is converted into the binary image.

For any pixel in an image, the sets of pixels that are connected to that pixel are called connected component of an image [17]. The analysis of connected components is mainly used for many automated image processing applications such as road map extraction, line detection, etc. Connected components of an image are extracted by using morphological operations. Let G is an image and connected components in an image are denoted as G(1), G(2), G(3),…. The first non-zero pixel in an image is represented as X_0. The connected pixels with this X_0 pixel are extracted as per the (1). That X_0 is dilated with structure element E and dilated output intersected with an image G that output is X_1. If $X_1 \neq X_0$ then this iteration process is repeated, if $X_1 = X_0$ then iteration is stopped and X_1 is the first set of the connected component. The above process is continued until all the non-zero pixels are grouped in any one of the connected components.

$$X_k=(X_{k-1} \oplus E) \cap G \qquad K=1,2,3,\ldots. \tag{1}$$

where $\oplus$ represents the morphological dilation and $\cap$ represents the intersection operation. Connected components are extracted from the resultant image of adaptive global thresholding. Some of these connected components are non-road regions and these unwanted components are removed by using the Trivial opening method. The trivial opening is used to extract the connected components based on some criteria. Let G be an image, $\{G(n)|n = 1, 2, 3, \ldots,N\}$ is a sequence of connected components in the image G which are extracted using (1). The trivial opening is defined with a condition T, as follows in Eq. (2).

$$\tau_0 = \begin{Bmatrix} G(i), \ if \ \ G(i) \ satisfy \ the \ condition \ T \\ \Phi, \ otherwise \end{Bmatrix} \tag{2}$$

where Ø represents the null set. Therefore, τ_0 is the trivial opening associated with condition T. If connected component satisfied the condition T, the entire region of that components is preserved. So shape and size are not disturbed by this opening. Road areas are easily filtered by trivial opening because roads have appeared as an identical region and long features in satellite images. The roads are extracted by selecting the condition as the long axes of a minimum ellipse for trivial opening operation. The Trivial opening for road detection is expressed as follows in Eq. (3).

$$R = \{G| \text{Long axis of axis of minimum ellipse enclosing } G(i) >= T\} \tag{3}$$

where G is an image and G(i) is connected components of an image. Thus, resultant image R has the connected components which are greater than T and this resultant image consists of road regions and all unwanted regions are removed. The resultant image of the trivial opening is in binary format which is converted into gradient format to extract the boundary of road network using SGW based approach. The gradient conversion is done using Eq. (4).

$$C(x, y) = R(x, y) \times G(x, y) \tag{4}$$

where R(x, y) is the resultant image of the trivial opening method, G (x, y) is an original satellite image and C(x, y) is converted gradient format image, and × represents the multiplication operation.

3.1. Road boundary extraction using SGW based Algorithm

The boundary of the road network is extracted with the help of Simplified Gabor Wavelet. One dimensional Gabor function is proposed by D. Gabor in 1946 and J. G. Daugman extended it to 2D later. A Gabor wavelet is described as a Gaussian kernel function modulated by a sinusoidal plane wave that has an optimal location in both the frequency domain and the space domain [18]. The GW is commonly used for extracting local features for various applications such as object detection, recognition and tracking8. The 2D Gabor wavelet is represented as in Eq. (5).

$$G(x, y, \theta, \sigma, \omega) = \exp[-\frac{x^2 + y^2}{2\sigma^2}]\exp[\, j\omega(x\cos\theta + y\sin\theta)] \tag{5}$$

where σ is the standard deviation of the Gaussian function in x- and y-directions, ω denotes the spatial frequency and θ adjust the orientation of the wave. The family of Gabor kernels is obtained for different spatial frequencies and orientations using (5). These kernels are used to extract features from an image. The edge features of an image are extracted using Gabor filter by 2D convolution of the input image I(x, y) and G(x, y) as in Eq. (6).

$$E(x, y) = I(x, y) \otimes G(x, y) \tag{6}$$

where ⊗ denotes the 2D convolution operation. The computation required for Gabor wavelet based feature extraction is very intensive. This is in turn, creates a bottleneck problem for real-time processing. Hence, an efficient method for extracting Gabor features is needed for many practical applications. Jiang et al. proposed that the imaginary part of a Gabor filter is an efficient and robust means for features extraction [8]. The imaginary part of a Gabor Wavelet is called as Simplified Gabor Wavelet (SGW) which is given in Eq. (7).

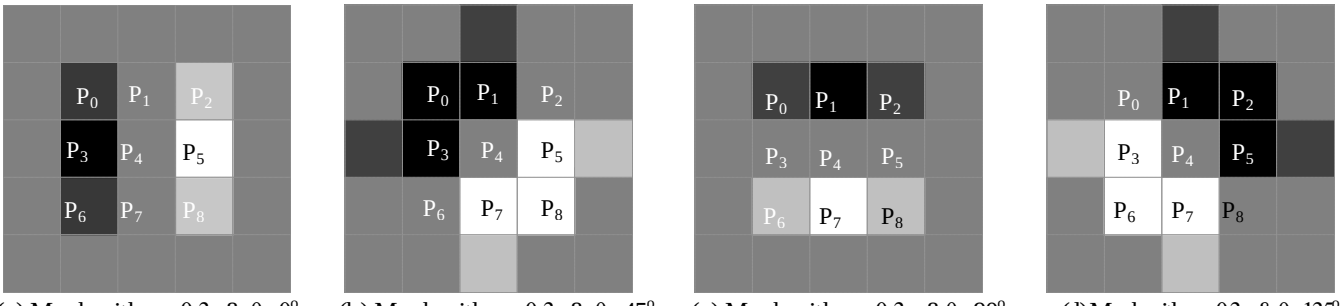
$$S(x, y, \theta, \sigma, \omega) = \exp[-\frac{x^2 + y^2}{2\sigma^2}]\sin[\omega(x\cos\theta + y\sin\theta)] \tag{7}$$

Set of Simplified Gabor kernels for different spatial frequencies (ω) and orientations (θ) is obtained using Eq. (7). These kernels are used to extract boundary of the road network. The values of GW are continuing one. Its values are quantized to a certain number of levels. The determination of the quantization levels R1 and R2 for an SGW is the same as that in [8].

The important parameters for the GWs or SGWs are the values of ω, σ, and θ which are used to determine the road network detection. The significance of Simplified Gabor Wavelet transform in edge feature extraction is explained by Sujatha and Selvathi [19]. The SGW based edge detection method yields an optimal result for two different scales (ω) and four different orientations (θ) which is already proved in [8] and [19]. The convolution of an SGW of scale ω and orientation θ with the image I(x,y) generates the SGW features and is denoted as $C_{\omega,\theta}(x, y)$. The SGW feature $C_{\omega,\theta}(x, y)$ is computed by convolving the image I(x, y) with the SGW $S_{\omega,\theta}(x, y)$ as given in Eq. (8).

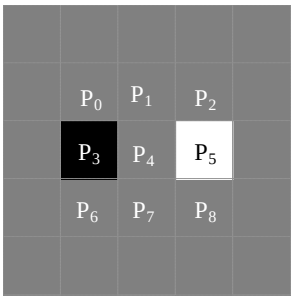
$$C_{\omega i,\theta j}(x, y) = I(x, y) \otimes S_{\omega i,\theta j}(x, y) \tag{8}$$

where $\omega_0 = 0.3\pi, \omega_1 = 0.5\pi$, and $\theta_j = j\pi/4$, for j = 0. . . 3. Thus, two different scales and four different orientations are adopted for this proposed work. The corresponding patterns of the eight SGWs are shown in Fig. 1.

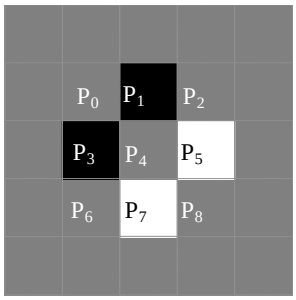


(a) Mask with ω=0.3π& θ=0° (b) Mask with ω=0.3π& θ=45° (c) Mask with ω=0.3π &θ=90° (d) Mask with ω=0.3π & θ=135°

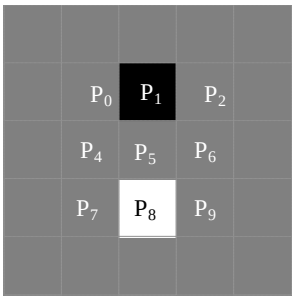
Fig. 1 Mask of the SGWs



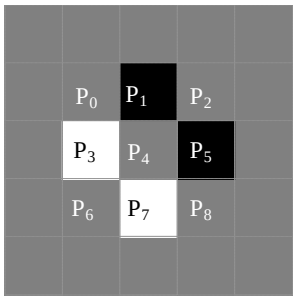
(e) Mask with ω=0.5π& θ=0°



(f) Mask with ω=0.5π & θ=45°



(g) Mask with ω=0.5π& θ=90°



(h) Mask with ω=0.5π& θ=135°

Fig. 1 Mask of the SGWs (continued)

Suppose an SGW pattern is moved to the pixel position (x_c, y_c), the computation of the output $C(x_c, y_c)$ of this position is computed as per the Table 1.

Table 1 SGW features for different values of ω and θ

ω	θ	SGW features	Figure
0.3π	0°	$C_1(x_c, y_c) = R_1(P_2 + P_8 - P_0 - P_6) + R_2(P_5 - P_3)$	1(a)
0.3π	45°	$C_2(x_c, y_c) = R_2(P_5 + P_7 + P_8 - P_0 - P_1 - P_3)$	1(b)
0.3π	90°	$C_3(x_c, y_c) = R_1(P_6 + P_8 - P_0 - P_2) + R_2(P_7 - P_1)$	1(c)
0.3π	135°	$C_4(x_c, y_c) = R_2(P_3 + P_6 + P_7 - P_1 - P_2 - P_5)$	1(d)
0.5π	0°	$C_5(x_c, y_c) = R_2(P_5 - P_3)$	1(e)
0.5π	45°	$C_6(x_c, y_c) = R_2(P_5 + P_7 - P_1 - P_3)$	1(f)
0.5π	90°	$C_7(x_c, y_c) = R_2(P_8 - P_1)$	1(g)
0.5π	135°	$C_8(x_c, y_c) = R_2(P_3 + P_7 - P_1 - P_5)$	1(h)

The resulting SGW feature $M_{\omega,\theta}(x, y)$ at a pixel position (x_c, y_c) is equal to the absolute maximum of the eight $C_{\omega,\theta}(x, y)$ and it is calculated as given in Eq. (9).

$$M_{\omega,\theta}(x_c, y_c) = \max\{(C_{\omega i,\theta j}(x_c, y_c),\ i = 0,1 \text{ and } j = 0,1,2,3)\} \tag{9}$$

where $\omega_0 = 0.3\pi, \omega_1 = 0.5\pi$, and $\theta_j = j\pi/4$, for $j = 0, \ldots, 3$. The absolute maximum $M_{\omega,\theta}(x, y)$ yields the boundary of the road network using Eq. (9).

3.2. Extraction of centerline of road network

The morphological thinning operation is applied to get the centerline of the road network. The thinning of an image G is defined by a structure element E as in Eq. (10).

$$G\Theta E = G - (G * E) = G \cap (G * E)^C \tag{10}$$

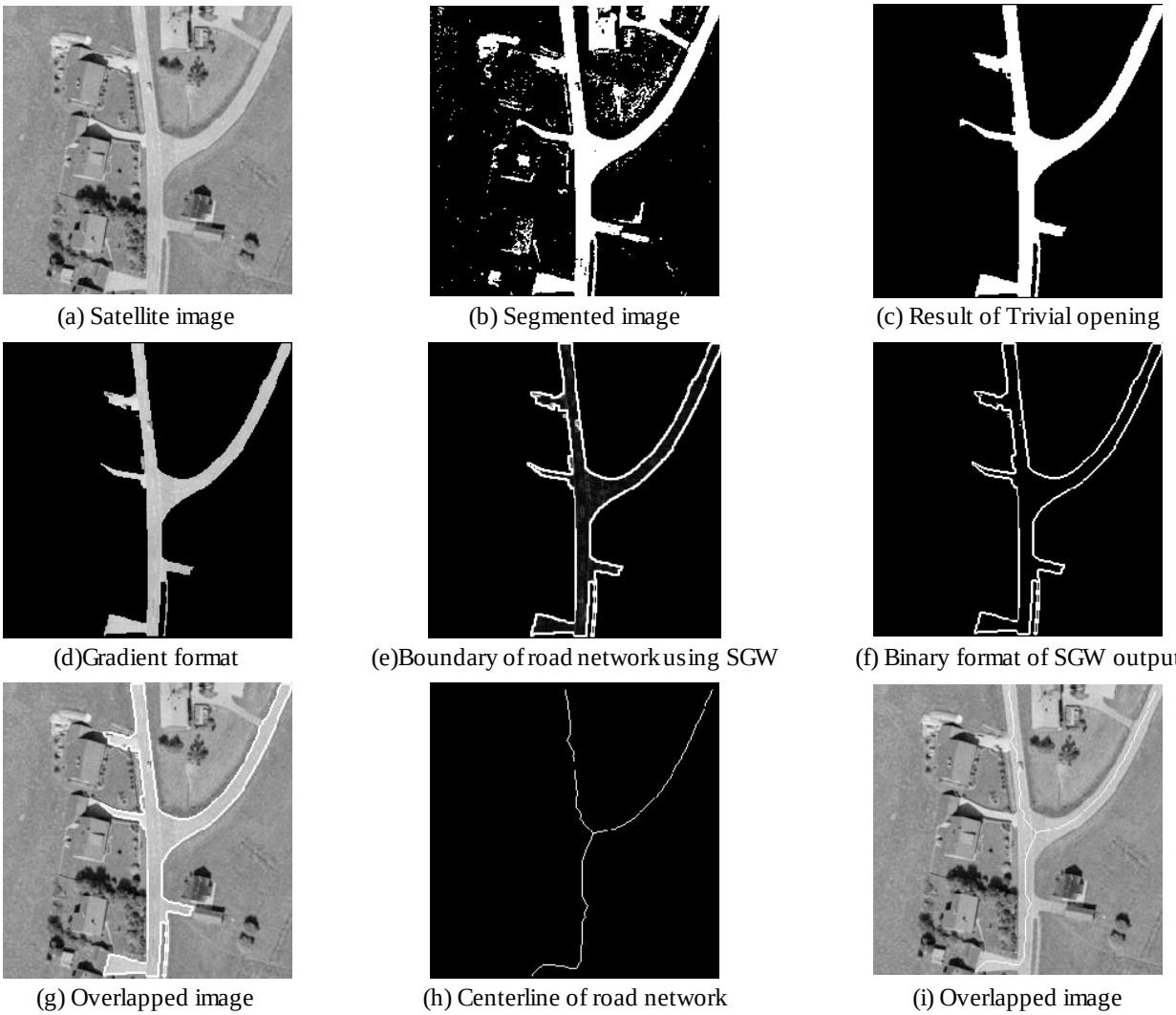
where Θ represents the morphological thinning operation, * represents the hit-or-miss transform and 'c' represents the complement function. The hit-or-miss transform is used to identify the specified configuration of pixels as given in Eq. (11).

$$G * E = (G\Theta E_1) \cap (G^c \Theta E_2) \tag{11}$$

where E1 & E2 are subsets of E related to the object and background, respectively. Thus, the centerline of the road network is extracted using the morphological thinning algorithm.

4. Results and Discussion

The proposed methodology is applied on satellite images collected from Satellite Imaging Corporation and Apollo Mapping [20-21]. The qualitative results of different steps of the proposed method for satellite image are given in Fig. 2.



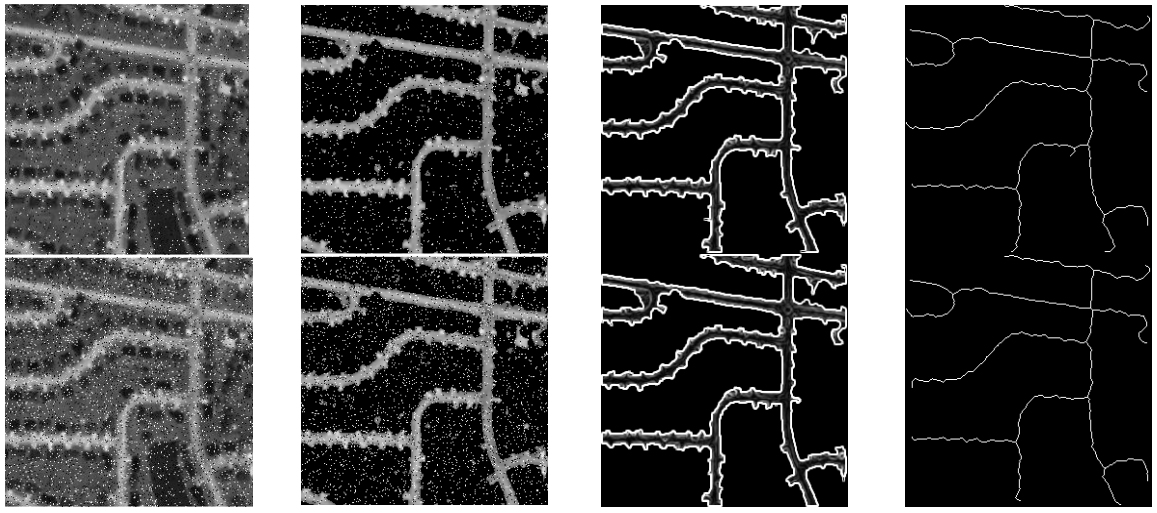
(a) Satellite image (b) Segmented image (c) Result of Trivial opening

(d)Gradient format (e)Boundary of road network using SGW (f) Binary format of SGW output

(g) Overlapped image (h) Centerline of road network (i) Overlapped image

Fig. 2 Results of SGW based road network extraction

The proposed work is implemented on noisy images at various noise density levels from 10% to 50% and the results are given in Fig. 3. Noisy images at various noise density levels, corresponding intermediate results are shown in Fig. 3. The final extracted road maps at all noise levels are almost equal to the noiseless result. Thus, this result shows that the proposed work produces road map output equal to noiseless image at the noise levels up to 50% and it proves that this work is insensitive to noises.



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Noise in % (a) Noisy Image (b) Result of trivial Opening (c) Result of Boundary detection (d) Final extracted road map

Fig. 3 Results of SGW based road network extraction in noisy images at various noise levels

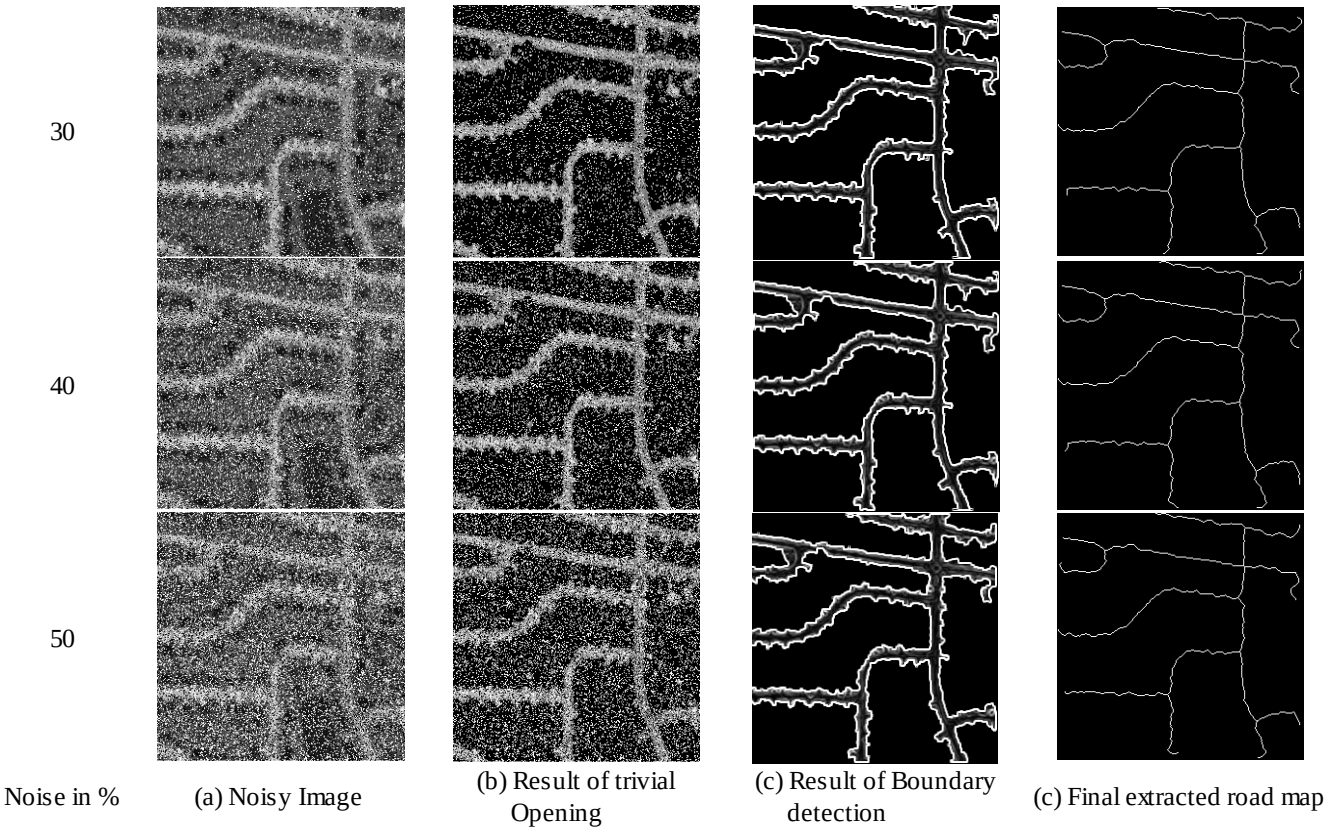


Fig. 3 Results of SGW based road network extraction in noisy images at various noise levels (continued)

5. Proposed FPGA Architecture for Road Network Extraction Using SGW

The FPGA architecture is proposed for extraction of road network boundary and centerline using SGW. For real-time application, hardware implementation is most needed. For FPGA implementation, the image must be converted into hexa data text file. The overall flow diagram of FPGA implementation of road network extraction is shown in Fig. 4.

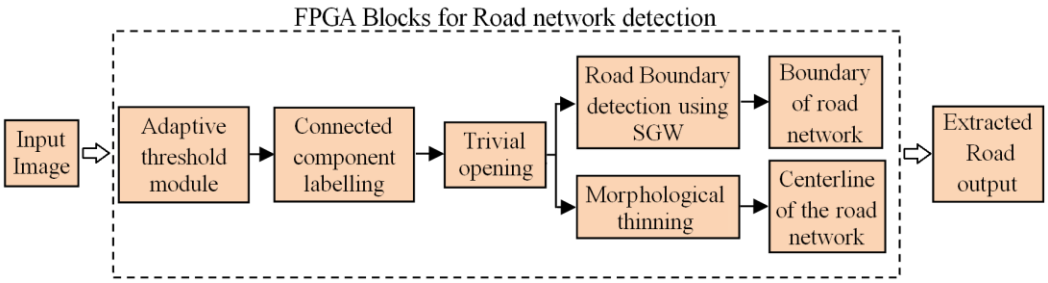


Fig. 4 Flow Diagram of FPGA implementation of proposed work

The Matlab program is used to convert the image data into hexa data file. FPGA architecture is designed to process these data and produces the output which is converted into image format by using Matlab program.

5.1. FPGA architecture for Road Network Extraction

The block diagram of the proposed FPGA architecture is shown in Fig. 4. It consists of adaptive threshold module, connected component labelling, trivial opening, SGW based approach for boundary detection, and morphological thinning. The input image is converted into binary using Gray to Binary converter (GTB) block and the threshold value is chosen using adaptive threshold method. The internal diagram for Gray to Binary converter (GTB) is given in Fig. 5. In this architecture, P is the 8-bit pixel value of an image and T is the 8-bit threshold value. The converted binary output contains some unwanted regions and is removed using connected component extraction. Connected components are extracted using (1).

Converted binary image from the above adaptive threshold method is assigned as matrix A. Any one of 3*3 structure element is chosen and assigned as B. The first non-zero element position in the input matrix A is found. 3*3 sized matrix X is initialized with zeros and 1 is placed in the non-zero element position found in the previous step. Morphological dilation using the structure element B on matrix X is performed. The dilated matrix is intersected with the matrix A and denoted as Y. If Y and X are not equal, then perform dilation and intersection again. If both are same, then iteration is stopped. The position of non-zero elements in the Y is labelled with number L. where L is the number of connected component in the image. Similarly, place zero in those positions in the input matrix A. The internal architecture of Connected Component Labelling Block (CCLB) is given in Fig. 6. The first non-zero block is followed by dilation block and it is used to find the maximum among the neighbors. The morphological dilation architecture and single bit maximum block (SMAX) is also included in Fig. 6.

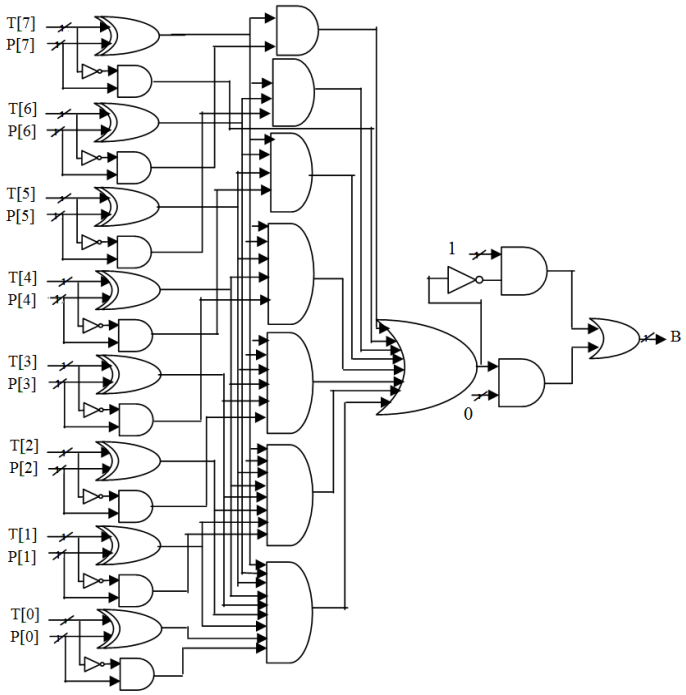


Fig. 5 Internal architecture of GTB

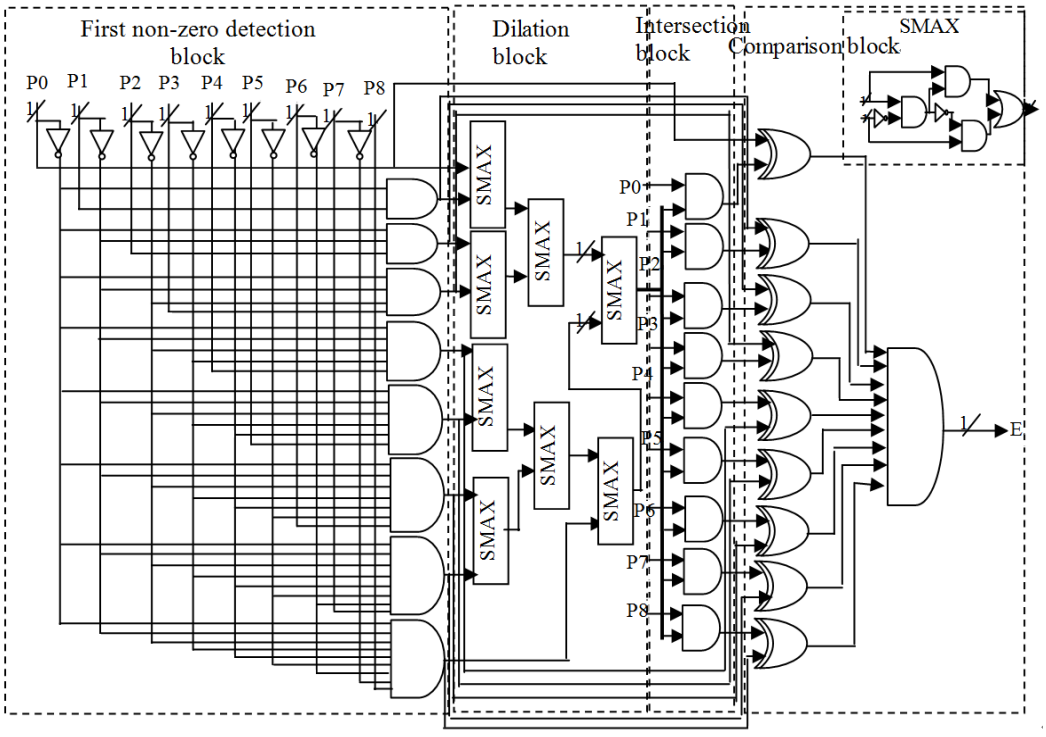


Fig. 6 Internal architecture for CCLB

By using these processes, the connected component is identified and an unwanted component is removed by using the trivial opening method. By using these processes, the connected component is identified and an unwanted component is removed by using the trivial opening method. In the trivial opening method, the length of each connected component is measured. Long length component is retained and the remaining is removed. These processes give the road region of the image. The resultant image of connected component extraction contains the road network region. The boundary of the road network is extracted using Simplified Gabor Wavelet based edge detection method. To apply the SGW, the resultant image is to be converted into the gradient format. The internal architecture of Binary to Gray conversion Block (BTGB) is shown in Fig. 7.

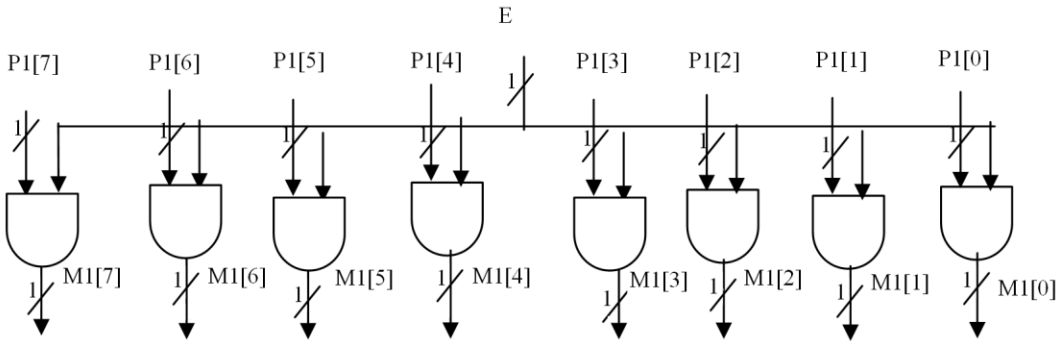


Fig. 7 Internal architecture for BTGB

The binary input pixel is single bit E. It is multiplied with 8-bit original pixel value and the 8-bit gradient pixel value is produced. If E is zero, the output pixel is zero. If E is one, then the output is equal to the original input value.

5.2. FPGA architecture for SGW based road boundary detection

The FPGA architecture for SGW based road boundary detection consists of eight convolution blocks (C1-C8), Maximum block and Gray to Binary (GTB) converter block. The detailed internal architecture of the SGW based road boundary detection is given in Fig. 8. The eight convolution blocks (C1-C8) are designed as per equations in Table 1. P0-P8 are the 8-bit pixels values and R1 & R2 are the quantization levels in SGW. Each convolution blocks need eight-bit adder (EADR), an eight-bit subtractor (ESUB) and eight-bit multiplication blocks. Maximum blocks are used to find the maximum value among the eight convolution outputs which give the gradient edge output. The Gray to Binary converter block (GTB) is already shown in Fig. 5. The internal architecture of Eight bit Adder (EADR), which consists of eight single bit adders (SADB), is shown in Fig. 9.

The internal architecture of Eight bit Subtractor (ESUB), which consists of eight single bit subtractor (FSUB), is presented in Fig. 10.

Multiplication block (MULB) is needed to multiply the two 8-bit numbers (X, Y). It produces 15-bit product output (P) and it is round off to 8-bit output (M). The internal architecture of MULB is shown in Fig. 11. The maximum blocks are used to find the maximum value of eight convolution outputs. Each maximum block (MAXB) is used to find the greater value between two inputs and its internal diagram is shown in Fig. 12.

Seven MAXB are needed to get maximum value among eight inputs and this maximum value is the gradient edge output. Gradient format output is converted into binary format by using GTB block which is presented in Fig. 5. This entire architecture provides the boundary of the road network. The centerline of that network is extracted using morphological thinning operations. The block diagram for morphological thinning is shown in Fig. 13 and internal architecture for thinning is shown in Fig. 14.

Thus, by using these architectures, road boundary and the centerline of the road network are extracted.

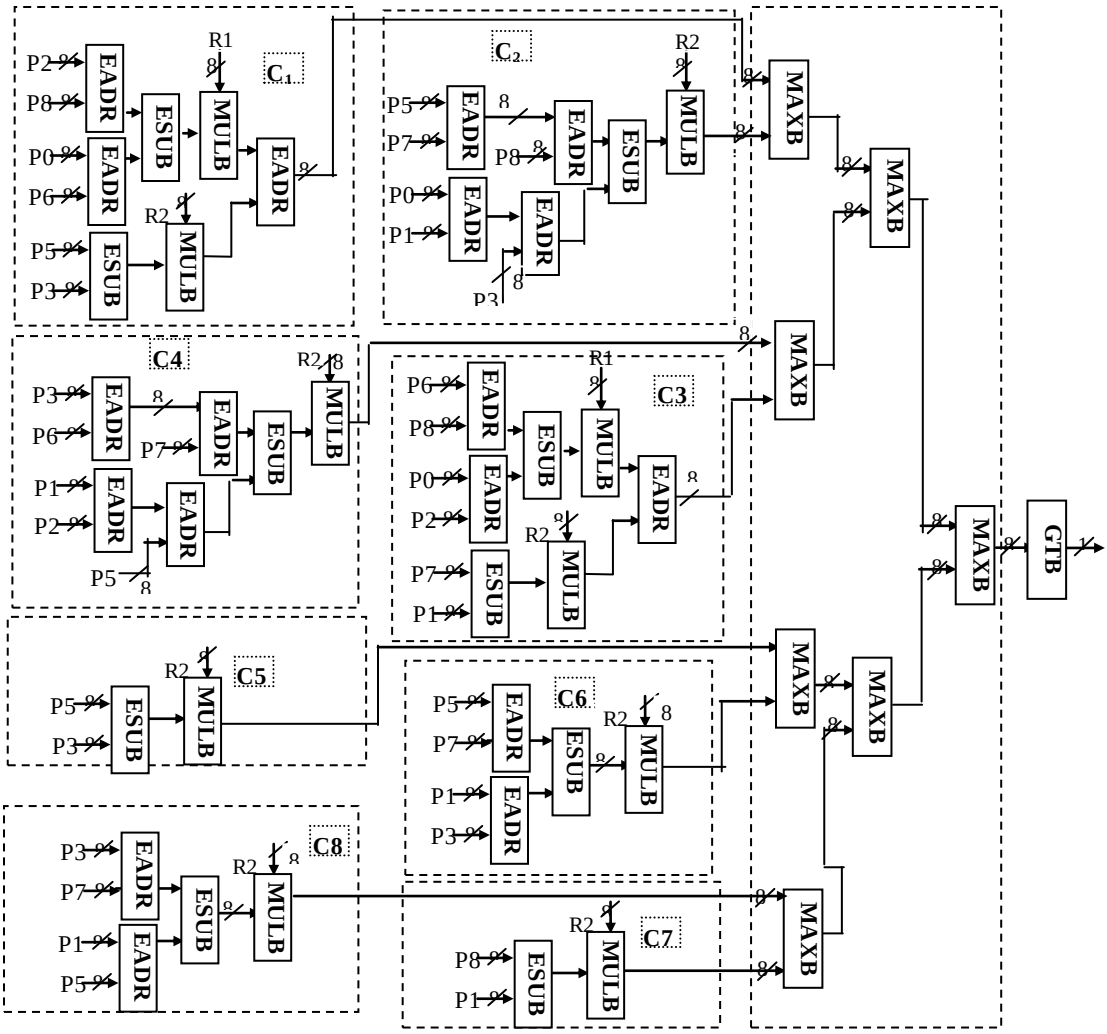


Fig. 8 Internal architecture of image edge detection using SGW

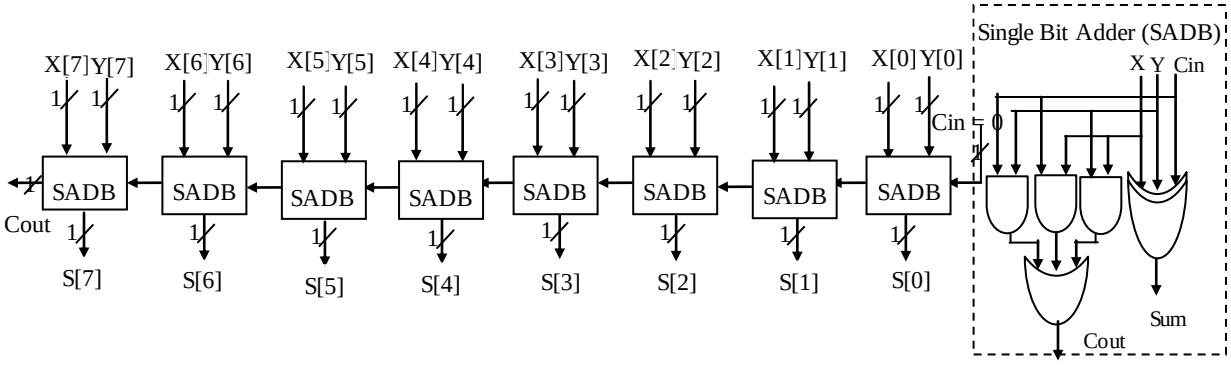


Fig. 9 Internal architecture of EADR

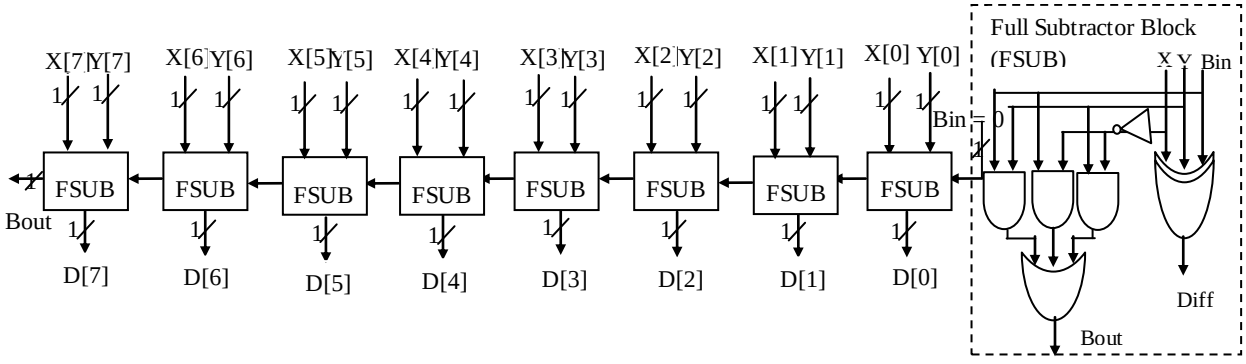


Fig. 10 Internal architecture of ESUB

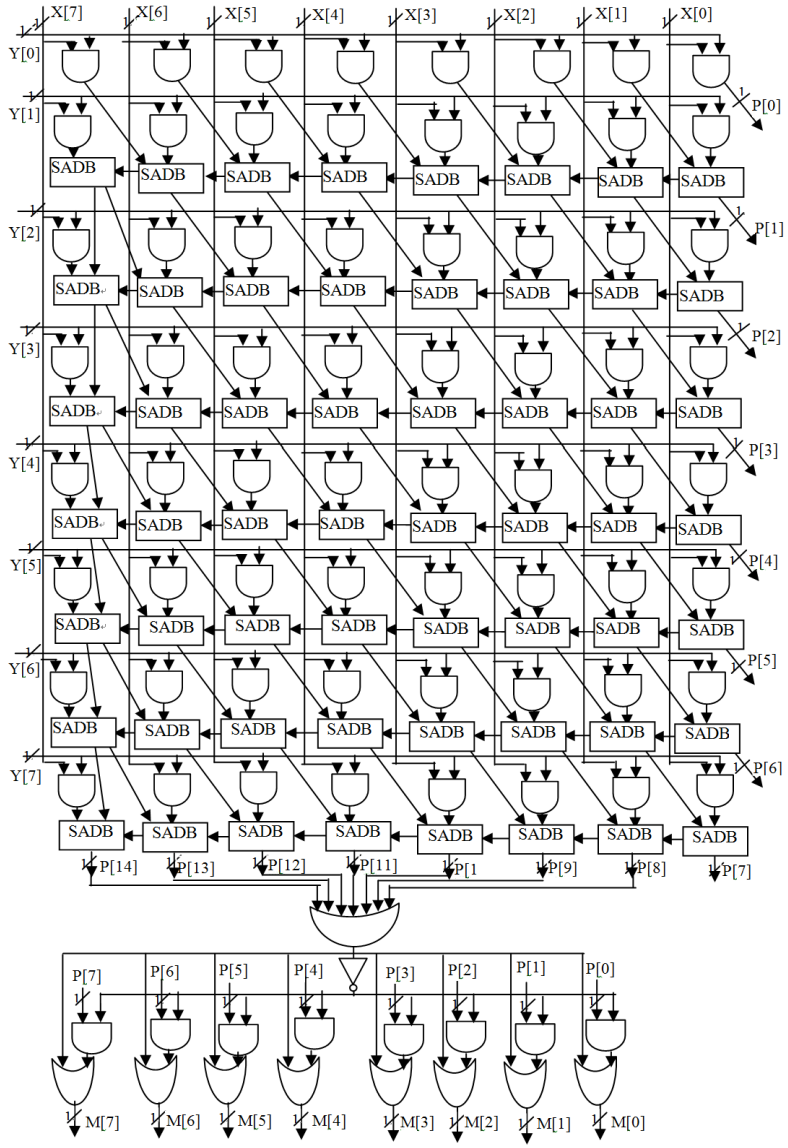


Fig.11 Internal architecture of MULB

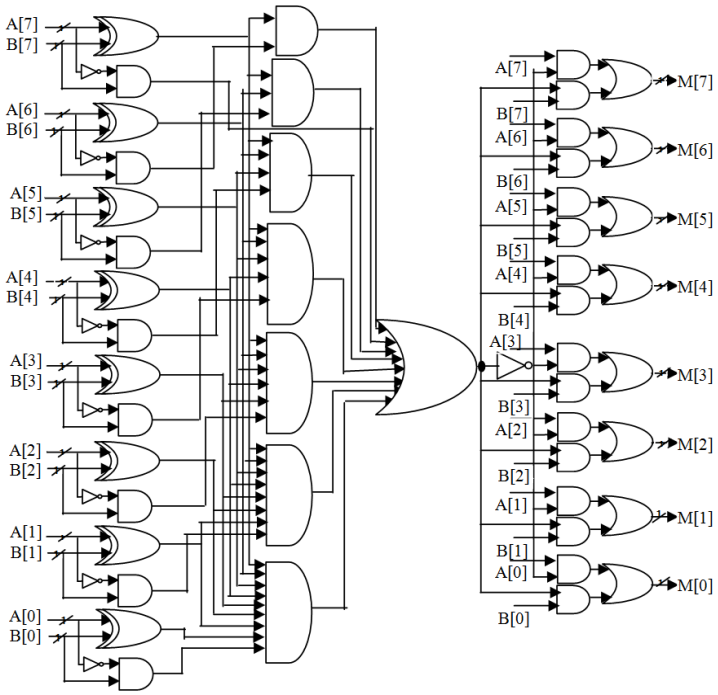


Fig. 12 Internal architecture of MAXB

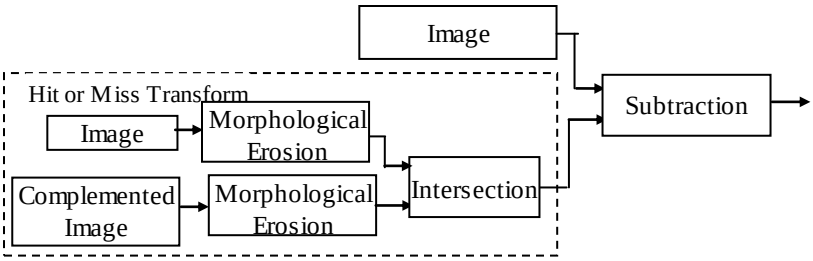


Fig. 13 Block diagram of morphological thinning

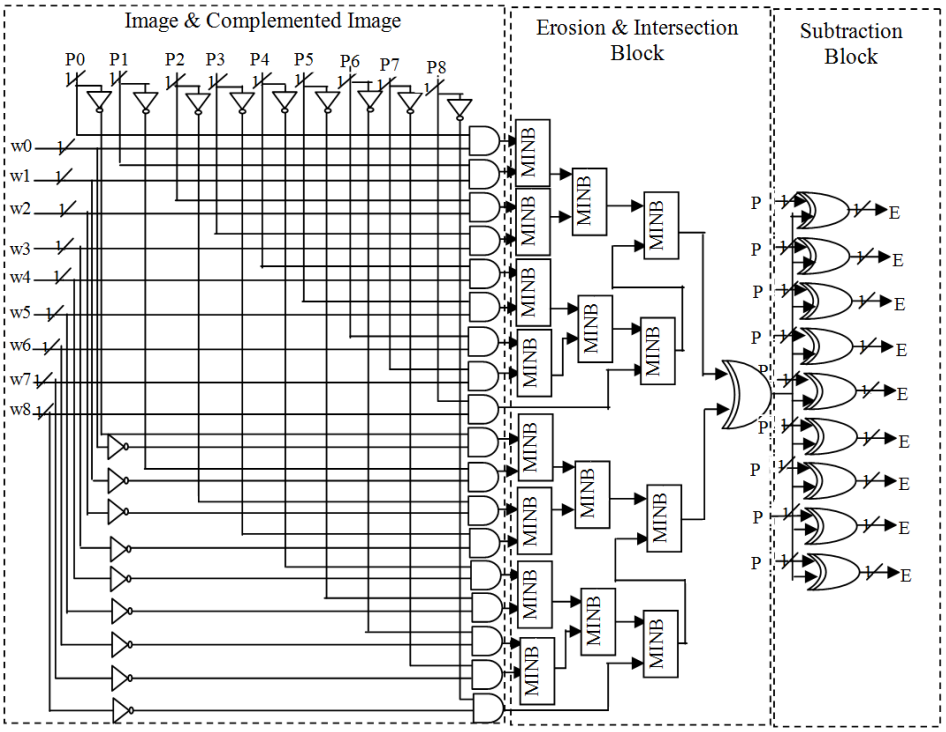


Fig. 14 Internal architecture of morphological thinning

6. FPGA implementation and synthesis results

The proposed architecture is implemented on a Xilinx Spartan 3 FPGA device. The sub-modules of the system are individually coded in Verilog and simulated using XilinxISE simulator. The RTL schematic of the architecture is given in Fig. 15.

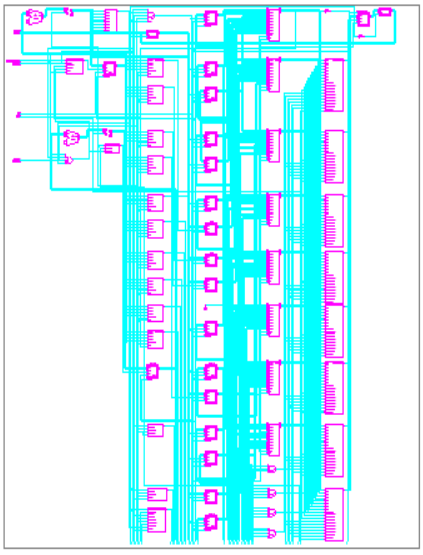


Fig. 15 RTL schematic of SGW based road network detection architecture

The synthesis and implementation in device Spartan 3, XC3S400TQ144 help to determine the resource utilization which indicates the number of resources exploited by the architecture. Table 2 shows the number of Flip-flops, LUT, Slice, and I/Os utilized.

Table 2 FPGA resource utilization and timing summary of proposed architecture

Slices	Slice Flip-Flops	4 input LUTs	IOBs	GCLKs	Minimum period	Maximum Frequency	Minimum input arrival time before clock	Maximum output required time after clock	Total memory usages
977/3584 (27%)	1148/7168 (16%)	1174/7168 (16%)	22/97 (22%)	1/8 (12%)	9.792ns	102.12MHz	8.768ns	7.165ns	215096 kb

The Table 2 proves that the proposed system requires very less area and only 16% of flip-flops, and 16% LUT are used. Thus, the proposed system provides better performance with less device utilization. The Timing Summary indicates that the minimum period required for implementing this architecture is 9.792 ns and the maximum frequency in which the design is operated in 102.12 MHz. The implemented device for the proposed image processing architecture in FPGA Editor shows the various programmable elements, which are called Configurable Logic Blocks containing flip-flops, latches and registers organized in slices as shown in Fig. 16.

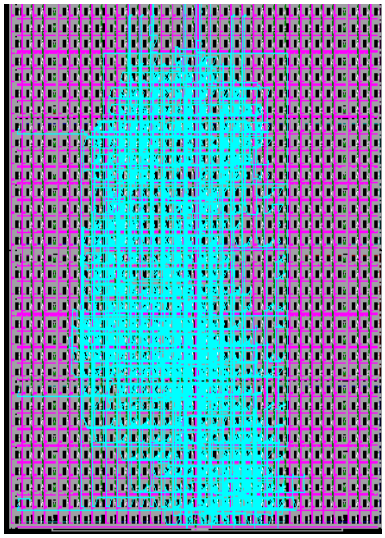


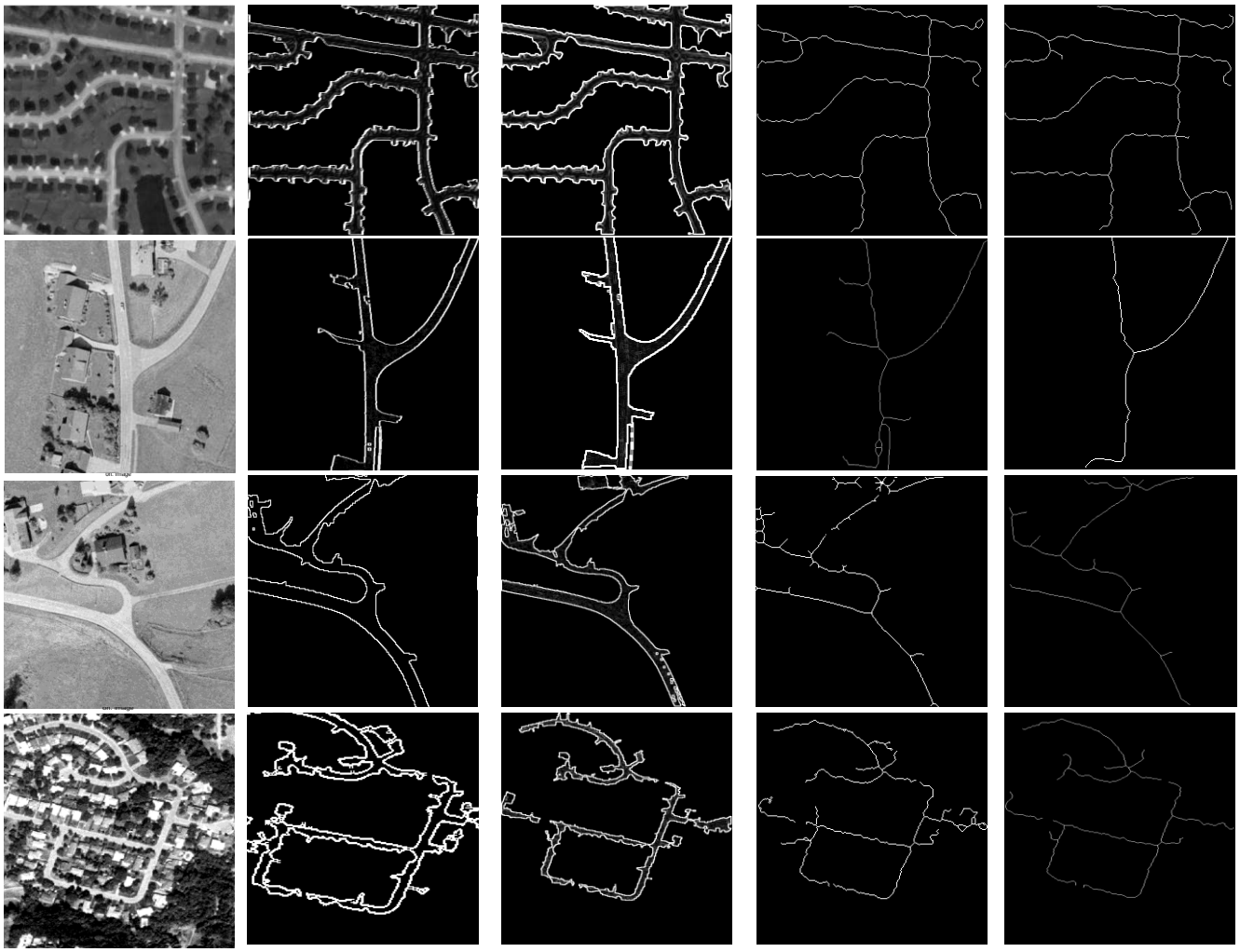
Fig. 16 Implemented devices in FPGA editor

The proposed hardware result is compared with other segmentation works. FPGA implementation of image segmentation work results are compared with proposed FPGA implementation of road segmentation results. These comparison values are tabulated in Table 3.

Table 3 Comparison of Device utilization report of proposed work with other segmentation works

Algorithm	#Slices	#Flip-Flops	#LUT	# IOB	Device
[22]	26%	18%	13%	65%	Spartan 3 XC3S50-5PQ208
[23]	11%	7%	9%	10%	Spartan3 XC3S200
[24]	14%	1%	10%	4%	Spartan XC3S200
[25]	9%	0%	9%	6%	Virtex 4 device XC4VLX200
[26]	37.3%	40.1%	47.3%	-	Virtex-5
[27]	4%	4%	3%	29%	Spartan XCSD3400A
[28]	48%	20%	52%	-	Virtex-5
Proposed system	**27%**	**16%**	**16%**	**22%**	**Spartan3 XC3S400-4TQ144**

The designed FPGA architectures for road boundary network extraction and centerline extraction are tested on satellite images and the obtained FPGA implementation results are compared with PC-based implementation results which are shown in Fig. 17.



(a) Satellite images

(b) FPGA Platform +Verilog

(c) PC platform + Matlab

(d) FPGA Platform +Verilog

(e) PC platform + Matlab

Boundary Extraction Results

Centerline Extraction Results

Fig. 17 Results of FPGA and PC based implementations of Road Network Extraction

Table 4 Comparison of Verilog and Matlab implementation results

Images	Algorithm	Completeness %	Correctness %	Quality %
Satellite image 1	Matlab	88.89	98.65	87.82
	Verilog	86.95	96.79	85.63
Satellite image 2	Matlab	89.21	98	87.61
	Verilog	87.52	97.93	85.86
Satellite image 3	Matlab	89.45	99.03	88.94
	Verilog	88.34	98.81	88.72
Satellite image 4	Matlab	91.29	95.70	85.96
	Verilog	89.13	93.92	83.28
Satellite image 5	Matlab	94.79	98.25	93.22
	Verilog	92.86	96.93	91.86

This comparison proves that Verilog implementation results are merely equal to Matlab implementation results. The performance of the road network detection is also analyzed quantitatively using various measures. Performance measures such as completeness, correctness, and quality are the most important parameters for the evaluation of the road extraction. The performance of hardware and software implementation of the proposed road extraction is observed by calculating these measures. The performance measures such as Completeness, Correctness, and Quality are evaluated for the proposed work on FPGA platform using Verilog and PC platform using Matlab. These results are tabulated in Table 4. In Matlab implementation, the

lowest value of completeness is 88.89 %, the maximum value is 94.78 % and correctness measures show that all the values are above 95.7 %. The quality measures lie between 85 % and 93% in Matlab implementation. The FPGA result is almost equal to Matlab implementation results. The performance measures are also evaluated for noisy images at various noise density levels and values are tabulated in Table 5.

Table 5 Performance measures of SGW based road network detection method for noisy images at various noise levels

noise Levels in %	Completeness %	Correctness %	Quality %
noiseless Image	89.45	99.03	88.94
5	89.45	99.03	88.94
10	89.45	99.03	88.94
20	89.42	98.98	88.91
30	89.4	98.96	88.89
40	89.39	98.95	88.86
50	89.38	98.95	88.84

The Table 5 shows that the maximum differences in completeness, correctness, and quality values are less than 1% with noiseless values. Thus, the proposed work is appropriate for road centerline detection in noisy images also. Table 6 shows the comparison of minimum, maximum and average values of completeness, correctness and quality measures of the proposed method with other methods. All the values in Table 5 are rounded to nearest integer. This table is plotted and is shown in Fig. 18. Thus, the comparisons in Table 6 and Fig. 18 prove that proposed method gives high results than other methods.

Table 6 Performance measures comparison of SGW based method with other methods

Methods	Completeness %			Correctness %			Quality %		
	Min	Max	Average	Min	Max	Average	Min	Max	Average
[9]	84	94	91	81	96	90	82	92	85
[10]	70	86	78	70	92	80	58	80	66
[11]	71	87	79	68	84	77	59	72	63
[12]	80	92	87	82	89	89	68	83	76
[13]	58	93	73	35	85	69	28	75	56
[14]	66	91	81	65	96	87	48	87	73
[16]	73	97	87	75	100	92	59	96	83
Proposed work	**89**	**95**	**91**	**96**	**99**	**98**	**86**	**93**	**89**

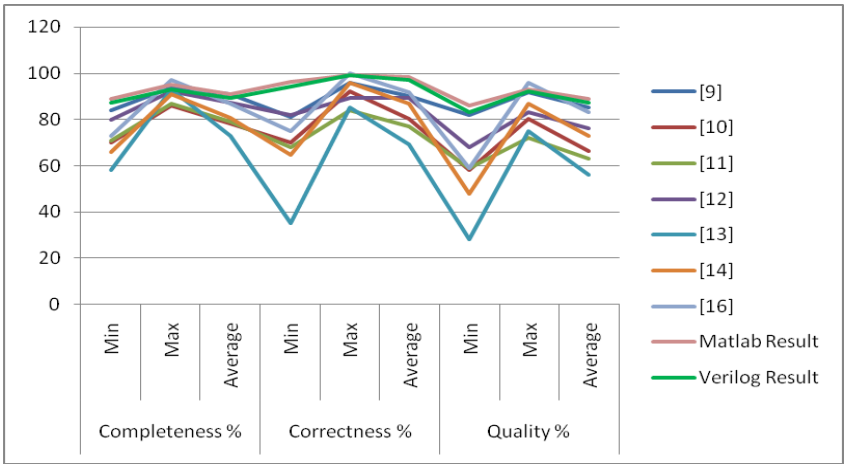


Fig. 18 Performance measures comparison plot of various methods with SGW based work

7. Conclusion

Road centerline extraction of high-resolution satellite images using Simplified Gabor wavelet is proposed in this work. The proposed work includes the following steps such as segmentation of approximated road regions using adaptive global threshold

method; trivial opening is applied to extract road pixels from the segmented region. SGW based approach is applied to detect the boundary of the road network. Thinning is applied to detect the centerline of the road network. FPGA architecture is proposed for this road network extraction. The designed architecture is simulated using Verilog, synthesized using Xilinx ISE. This architecture is implemented on Spartan 3 XC3S400-4TQ144 device. The device utilization is very less and time delay is 9.792ns (5.052ns logic, 4.74ns route). The total memory required for implementation of the developed method has been found as 215096 kilobytes. This architecture uses only 16% slice FFs on Xilinx Spartan 3 XC3S400-4TQ144. The proposed method is implemented on various satellite images and results in both Matlab and Verilog implementations are given. The completeness, correctness, and quality measures are evaluated for both implementations and results are compared. The FPGA -based implementation results are comparable with PC-based implementation results.

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