A Novel Absolute Sine-Carrier PWM-Based Discontinuous Space Vector Modulation for Vienna Delta-Switch Rectifiers with Comparative Performance Evaluation

Kanyarat Ek-iam [1], Prapawan Pangsri[2], Ong-ard Tubburee[1,*]

[1]Department of Industrial Electrical Technology, Faculty of Industrial Technology, Valaya Alongkorn Rajabhat University under the Royal Patronage, Pathum Thani, Thailand

[2]Department of Industrial Engineering Management, Faculty of Industrial Technology, Valaya Alongkorn Rajabhat University under the Royal Patronage, Pathum Thani, Thailand

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Abstract

This paper proposes an absolute sine-carrier pulse-width modulation (ASC-PWM) integrated with a discontinuous space-vector modulation (DSVM) framework for Vienna delta-switch rectifiers, aiming to improve input-current quality and harmonic performance while maintaining simplicity of implementation. The absolute sinusoidal carrier reshapes the pulse distribution while preserving the simplicity of comparator-based PWM. Closed-form dwell-time expressions and sector-dependent switching-state remapping are derived under unidirectional current-flow constraints. A voltage-oriented control (VOC) scheme is employed for DC-link regulation and power factor correction. Simulation results for a 230-V/50-Hz grid-connected system at 2.5 kHz demonstrate that the proposed method achieves lower total harmonic distortion of the input current and a higher power factor than the triangular, symmetrical sine, and inverted sine carriers. Although the proposed strategy yields a lower DC-link voltage due to reduced duty cycle, it provides superior harmonic performance with stable voltage regulation, making it suitable for high-power grid-connected rectifiers that prioritize input power quality.

Keywords: Vienna delta-switch rectifiers, absolute sine carrier, SVPWM, modulating signals, THD

1. Introduction

Three-phase pulse-width modulation (PWM) rectifiers are widely employed in modern power conversion systems due to their capability to regulate DC-link voltage and improve input power quality through switching control [1-2]. Compared with multilevel structures, three-phase two-level rectifiers are often preferred in medium-voltage applications because of their simpler topology, reduced semiconductor count, lower conduction and switching losses, and the absence of DC-link capacitor voltage imbalance issues [3-4]. Structurally, three-phase two-level rectifiers can be implemented in three main configurations: the Vienna wye-switch, Vienna delta-switch, and Vienna bridge-switch. Among these configurations, the Vienna delta-switch rectifier, as shown in Fig. 1, exhibits superior performance. It offers lower conduction and switching losses, as well as reduced total harmonic distortion (THD) of the input current [5-6], making it suitable for high-efficiency and compact designs.

Although many modulation and control schemes have been extensively investigated, achieving high-quality input current while maintaining low switching losses remains challenging. Existing PWM strategies often involve trade-offs between harmonic performance and implementation complexity. This motivates the development of more efficient modulation techniques that further improve input-current quality without increasing control complexity.

* Corresponding author. E-mail address: ongart.tub@vru.ac.th

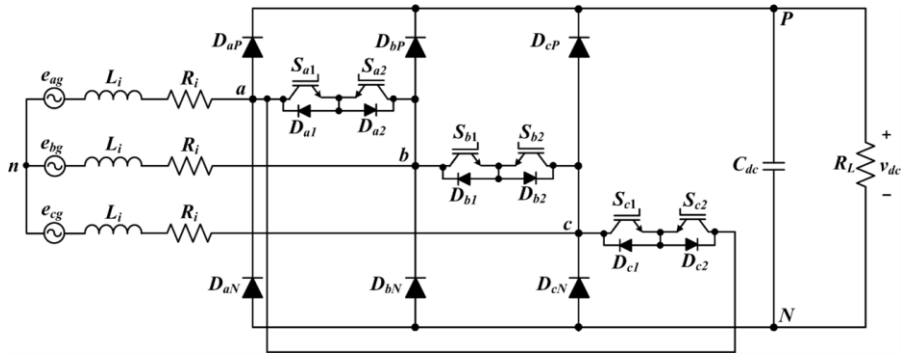


Fig. 1 Topological structure of the Vienna delta-switch rectifier

Various discontinuous switching strategies have also been proposed to further minimize switching losses by appropriately arranging switching sequences [7-8]. However, despite these advancements, reported experimental and simulation results indicate that many existing approaches still suffer from degraded input power quality, particularly in terms of high input current harmonic distortion. Such inadequate shaping of input currents leads to higher harmonic distortion and lower power factor, which in turn increase grid-side losses and impose additional stress on grid infrastructure [9]. To solve these problems, several modulation methods have been proposed, such as carrier-based PWM (CB-PWM), selective harmonic elimination PWM (SHE-PWM), and space vector modulation (SVM) [10-13].

Despite the simplicity and implementation advantage that CB-PWM offers, it suffers from limited DC-link voltage utilization and produces clustered harmonic spectra. In contrast, the SVM method improves both voltage utilization and harmonic performance; however, it generally requires sector identification and duty-cycle calculations, which increase implementation complexity. Carrier-based space vector PWM (SVPWM) has therefore emerged as a practical compromise, combining SVM performance with comparator-based simplicity [14].

Although carrier-based SVPWM techniques for Vienna rectifiers have been extensively studied, several critical gaps remain. Existing DSVM and carrier-based approaches predominantly rely on conventional triangular carriers (TC) or modulation-signal modification strategies, without explicitly considering carrier-shape engineering as a means of improving harmonic performance. For instance, recent work in [15] has addressed performance improvement through modulation-signal offset injection within a 12-sector SVPWM framework for Vienna rectifiers. However, this approach operates at the modulation-signal level and does not investigate how carrier waveform shaping influences switching behavior and harmonic performance. As a result, the potential of carrier-level design as an independent degree of freedom remains underexplored.

In practice, most carrier-based approaches rely on conventional triangular carriers. Alternative carrier-shaping techniques have been extensively investigated in inverter applications, where waveform shaping significantly influences harmonic performance [16]. For example, trapezoidal-triangular-carrier PWM (TTC-PWM) and symmetrical sine-carrier PWM (SSC-PWM) improve harmonic characteristics but at the cost of increased mathematical complexity or reliance on precomputed switching angles [17-19]. Inverted sine-carrier PWM (ISC-PWM) enhances spectral performance within specific modulation ranges; however, its effectiveness degrades at high modulation indices and typically requires half-cycle carrier inversion, thereby increasing implementation complexity [20-22].

An alternative yet largely unexplored approach is the use of an absolute sine-carrier PWM (ASC-PWM), which is obtained from the absolute value of a sinusoidal waveform. Unlike TC- or ISC-PWM, the ASC-PWM inherently provides a nonlinear yet smooth time mapping within each switching period without requiring polarity inversion. This valley-centered redistribution of switching instants has the potential to enhance harmonic spreading while preserving comparator-based simplicity. A targeted review of recent literature on Vienna rectifier modulation has been conducted, including carrier-based SVPWM, DSVM, modulation-signal offset methods, and alternative carrier-shaping techniques [14-22]. The results indicate that the integration of an analytically defined ASC-PWM with DSVM for the Vienna delta-switch rectifier has not been explicitly reported.

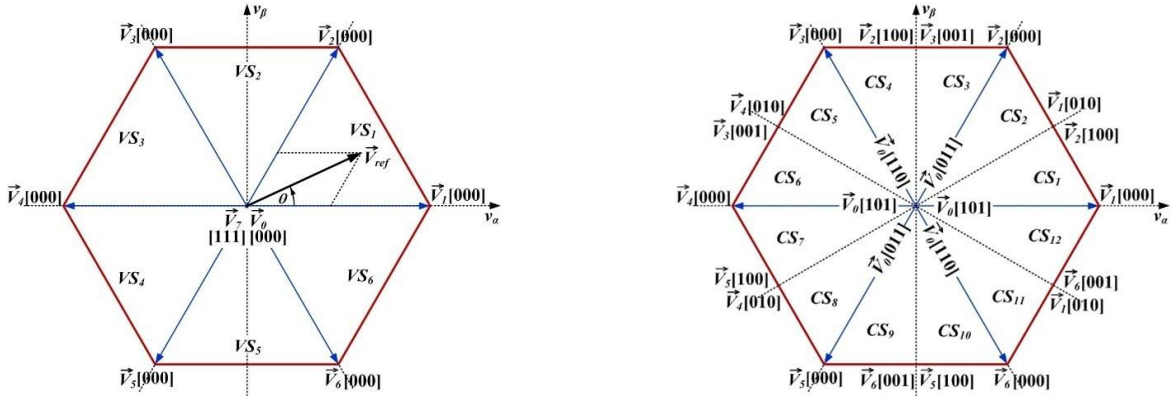
To address this research gap, this paper proposes an analytically defined ASC-PWM integrated with DSVM for the Vienna delta-switch rectifier. Unlike existing carrier-based approaches, the proposed method provides both analytical and implementation-level advantages. It employs a closed-form nonnegative carrier that can be generated in real time using a single sine evaluation and an absolute-value operation. In addition, it establishes a direct analytical relationship between the nonlinear carrier slope and valley-centered switching redistribution. The proposed scheme preserves conventional comparator-based implementation without requiring polarity inversion or complex logic, while enabling stable operation over a wider modulation-index range. Comprehensive simulations are conducted to evaluate input current quality, DC-link voltage regulation, and harmonic performance, with direct comparison to the TC-PWM, SSC-PWM, and ISC-PWM-based schemes.

2. Operational Analysis of the Vienna Delta-Switch Rectifier Based on SVM

Under the conventional SVM framework, the reference voltage vector (V_{ref}) is synthesized within a space vector plane divided into six equal regions, referred to as voltage sectors (VS_k = 1, 2, …, 6), as shown in Fig. 2(a). In each sector, the reference voltage vector is generated by two adjacent active vectors and two zero vectors, each associated with a specific three-phase switching state that produces balanced inverter output voltages.

For the Vienna delta-switch rectifier, the operating region is further partitioned into twelve equal intervals in the space vector diagram to accommodate the unidirectional current-flow constraint of the topology. Each interval is equivalent to half of a normal voltage sector and is referred to as a current sector (CS_n, n = 1, 2, …, 12), thereby increasing the resolution of sector division for current-direction control. Accordingly, the switching states within each current sector must be redefined from their conventional inverter representations. For example, in the current sector CS_1 (corresponding to voltage sector VS_1), the active vectors V_1 and V_2 are used, while their states of switching are redefined from [1 0 0] and [1 1 0] to [0 0 0] and [1 0 0], respectively, thereby altering the current conduction paths. Similarly, it is also true for CS_2 that the switching states of V_1 and V_2 are changed as [0 1 0] and [0 0 0], respectively. This sector-based remapping ensures accurate mapping of input current conduction paths while maintaining the desired DC output polarity and guarantees consistent rectifier operation under different current directions.

The zero-vector states are determined by the input currents that flow in the surviving two-phase circulating path, which does not provide power to the DC load. Accordingly, the zero vector V_0 is reassigned to [1 0 1] in current sector CS_1 and [0 1 1] in current sector CS_2, thereby enabling internal current circulation during zero-vector intervals. By applying this procedure systematically, the modified switching states for both active and zero vectors are obtained for all twelve current sectors. The complete switching-state mapping is summarized in Fig. 2(b), ensuring that the modulation scheme remains consistent with the rectifier's unidirectional current-flow constraint across all operating sectors.



(a) Conventional voltage sector and switching states

(b) Current sector and modified switching states for the Vienna delta-switch

Fig. 2 Two-level SVM diagrams

3. Command Signal Design Based on Nearest Three Vectors

Within each current sector, the rotating reference voltage vector is synthesized using the two adjacent active vectors and one zero vector, following the conventional six-voltage-sector SVM framework. As an example, consider current sector CS_1, where the reference voltage vector is formed from vectors V_1, V_2, and V_0:

$$\vec{V}_{ref} = \frac{t_1}{T_S}\vec{V}_1 + \frac{t_2}{T_S}\vec{V}_2 + \frac{t_0}{T_S}\vec{V}_0 \tag{1}$$

where T_s represent the switching period, and t_1, t_2, and t_0 denote the dwell times of vectors V_1, V_2, and V_0, respectively. These dwell times depend on the angular position (θ) of the reference voltage vector and the modulation index (m_a):

$$t_1 = T_S m_a \cos\left(\pi/6 + \theta\right),\ t_2 = T_S m_a \cos\left(\pi/2 - \theta\right),\ t_0 = T_S - t_1 - t_2 \tag{2}$$

For a two-level SVM, the modulation index is defined as the normalized magnitude of the reference voltage vector with respect to the DC-link voltage (V_{dc}), which serves as a key parameter for quantifying voltage utilization and determining the operating range of the converter:

$$m_a = \frac{\sqrt{3}V_{ref}}{V_{dc}} \tag{3}$$

According to the two-level SVPWM principle, the phase-modulating signals are obtained by normalizing the conduction intervals of the nearest three vectors (NTVs) to the switching period. A symmetrical discontinuous sequence is adopted to ensure that only one phase leg commutates at a time, thereby reducing switching losses. For current sector CS_1, the five-vector sequence $V_1V_2V_0V_2V_1$ yields the switching pattern [0 0 0]-[1 0 0]-[1 0 1]-[1 0 0]-[0 0 0], from which the normalized phase references are:

$$v_{a,ref} = \frac{t_0 + t_2}{T_S} = 1 - m_a \cos\left(\theta + \pi/6\right),\ v_{b,ref} = \frac{0}{T_S} = 0,\ v_{c,ref} = \frac{t_0}{T_S} = 1 - m_a \cos\left(\theta - \pi/6\right) \tag{4}$$

When the reference voltage vector moves to the current sector CS_2, the vector sequence remains $V_1V_2V_0$, but the vector switching states are inverted to satisfy the sector-specific current condition. The resulting pattern [0 0 0]-[0 1 0]-[0 1 1]-[0 1 0]-[0 0 0] leads to:

$$v_{a,ref} = \frac{0}{T_S} = 0,\ v_{b,ref} = \frac{t_0 + t_1}{T_S} = 1 + m_a \cos\left(\pi/2 + \theta\right),\ v_{c,ref} = \frac{t_0}{T_S} = 1 - m_a \cos\left(\theta - \pi/6\right) \tag{5}$$

Applying the same analytical procedure yields the dwell-time relations and modulation equations for the remaining current sectors. As observed from Table 1, although each current sector corresponds to different switching sequences and current polarities, every two consecutive sectors share identical modulation signal expressions. Consequently, only six distinct modulation patterns are sufficient to represent all twelve current sectors, thereby reducing memory requirements and computational burden in practical digital control systems.

Table 1 Three-phase modulation signal equations for all current sectors

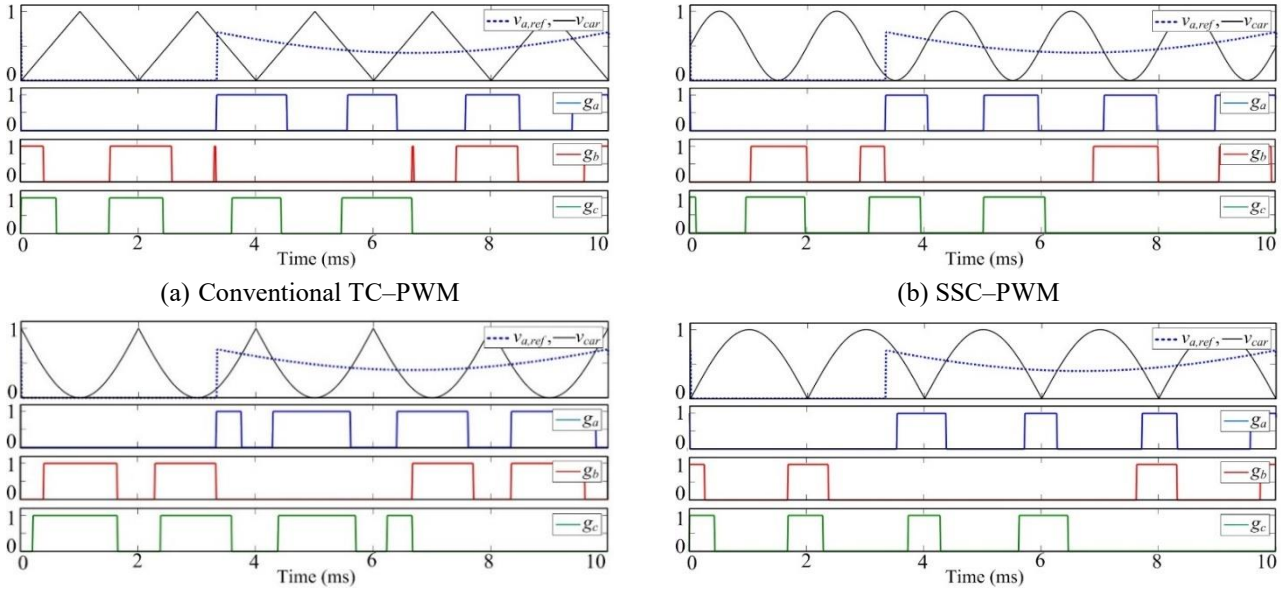
Current sectors	Modulation signal equations	Current sectors	Modulation signal equations
1 and 12	$v_{a,ref} = 1 - m_a \cos\left(\theta + \pi/6\right),\ v_{b,ref} = 0,$ $v_{c,ref} = 1 - m_a \cos\left(\theta - \pi/6\right)$	6 and 7	$v_{a,ref} = 1 + m_a \cos\left(\theta + \pi/6\right),\ v_{b,ref} = 0,$ $v_{c,ref} = 1 + m_a \cos\left(\theta - \pi/6\right)$
2 and 3	$v_{a,ref} = 0,\ v_{b,ref} = 1 + m_a \cos\left(\pi/2 + \theta\right),$ $v_{c,ref} = 1 - m_a \cos\left(\theta - \pi/6\right)$	8 and 9	$v_{a,ref} = 0,\ v_{b,ref} = 1 + m_a \cos\left(\theta - \pi/2\right),$ $v_{c,ref} = 1 + m_a \cos\left(\theta - \pi/6\right)$
4 and 5	$v_{a,ref} = 1 + m_a \cos\left(\theta + \pi/6\right),$ $v_{b,ref} = 1 + m_a \cos\left(\pi/2 + \theta\right),\ v_{c,ref} = 0$	10 and 11	$v_{a,ref} = 1 - m_a \cos\left(\theta + \pi/6\right)$ $v_{b,ref} = 1 + m_a \cos\left(\pi/2 - \theta\right),\ v_{c,ref} = 0$

4. Proposed ASC-PWM Scheme

In carrier-based PWM, the switch driving signal is generated by comparing the normalized modulating signal $v_{i,ref}$ ($i \in \{a, b, c\}$) with a periodic carrier waveform v_{car} at the switching frequency f_{sw} ($T_S = 1/f_{sw}$), as shown in Fig. 3. The binary switching function of each phase leg is defined as:

$$g_i(t) = \begin{cases} 1, & v_{i,ref} \geq v_{car} \\ 0, & v_{i,ref} < v_{car} \end{cases} \tag{6}$$

The resulting signal $g_i(t)$ is mapped to the corresponding controllable power switches (S_{i1}, S_{i2}) based on the current-sector switching table of the Vienna delta-switch rectifier. Hence, the proposed method preserves the conventional comparator-based structure, while the contribution is realized through carrier reshaping.



(a) Conventional TC–PWM (b) SSC–PWM

(c) ISC–PWM (d) Proposed ASC–PWM

Fig. 3 Comparison of carrier-based PWM schemes showing the a-phase modulating signal and corresponding three-phase switch driving signals (f_{sw} = 500 Hz)

4.1 ASC definition

In the proposed approach, the ASC is constructed by taking the absolute value of a sinusoidal waveform and normalizing it within the same range [0, 1], consistent with conventional carrier amplitudes. The analytical expression of the proposed carrier is defined as:

$$v_{car}(t) = \left|\sin\left(\tfrac{1}{2}\omega_{sw}t\right)\right|, \quad 0 \leq t < T_S \tag{7}$$

where $\omega_{sw} = 2\pi f_{sw}$. Since the absolute operation doubles the waveform periodicity, the angular frequency is halved in Eq. (7) to maintain the carrier frequency equal to the switching frequency, thereby ensuring a fair comparison with TC and SSC carriers. The ASC is inherently nonnegative and can be generated in real time using a single sine function and absolute operator, avoiding the half-cycle polarity inversion required by ISC.

4.2 Nonlinear time mapping and pulse redistribution

The ASC introduces a nonlinear yet smooth temporal mapping within each switching period. Its slope is presented as:

$$\frac{d}{dt}\left|\sin\left(\tfrac{1}{2}\omega_{sw}t\right)\right| = \frac{1}{2}\omega_{sw}\,\mathrm{sgn}\left(\sin\left(\tfrac{1}{2}\omega_{sw}t\right)\right)\cos\left(\tfrac{1}{2}\omega_{sw}t\right), \tag{8}$$

where sgn(·) denotes the sign function. From Eq. (8), it can be observed that the effective carrier slope is small near the "valley" region (where $|\sin(\cdot)| \approx 0$) and larger near the "peak" region (where $|\sin(\cdot)| \approx 1$). As a result, for a given modulating level $v_{i,ref}$, the switching instants differ from those obtained with TC-PWM or SSC-PWM technique, leading to a modified pulse-spacing profile. When combined with DSVM-derived modulating signals, this nonlinear carrier slope provides a pulse distribution that better aligns with the sector-based dwell-time allocation. The resulting valley-centered pulse redistribution promotes improved harmonic spreading by shifting spectral energy toward higher frequencies.

4.3 Effect of carrier-based duty cycle on DC-link voltage

As illustrated in Fig. 3, the switching signals generated by different carrier waveforms exhibit distinct pulse distribution characteristics, which directly influence the effective duty cycle and energy transfer to the DC link. In carrier-based PWM, the switching function is defined by Eq. (6), and the corresponding average duty cycle ($\overline{d_i}$) within one switching period (T_S) can be expressed as:

$$\overline{d_i} = \frac{1}{T_S}\int_0^{T_S} g_i(t)\,dt, \tag{9}$$

For the conventional TC–PWM and SSC–PWM shown in Fig. 3(a) and Fig. 3(b), the carrier waveforms provide a relatively uniform pulse distribution, resulting in consistent energy transfer characteristics to the DC link. In contrast, the ISC–PWM in Fig. 3(c) exhibits pulse clustering near the switching boundaries, which may degrade harmonic performance without significantly reducing voltage utilization. However, as shown in Fig. 3(d), the proposed ASC–PWM introduces a valley-centered pulse redistribution due to its nonlinear carrier profile. This results in a reduced average duty cycle, as described below:

$$\overline{d}_{ASC} < \overline{d}_{TC,SSC,ISC} \tag{10}$$

Eq. (10) shows that the reduced duty cycle directly limits the energy transferred to the DC-link capacitor per switching period. The DC-link voltage dynamics are governed by the capacitor equation, which can be expressed as:

$$C\frac{dv_{dc}(t)}{dt} = i_{dc}(t) - i_{load}(t) \tag{11}$$

Under steady-state conditions, $i_{dc}(t) = i_{load}(t)$. Thus, a reduction in the average input current contribution (due to reduced duty cycle) may lead to a lower equilibrium DC-link voltage:

$$V_{dc}^{ASC} < V_{dc}^{TC,SSC,ISC} \tag{12}$$

The proposed ASC-PWM introduces a nonlinear pulse redistribution mechanism that tends to reduce the effective duty cycle of active switching states. This directly limits the energy transfer to the DC-link capacitor per switching cycle, which may result in a lower steady-state DC-link voltage. From an application perspective, this characteristic may limit the applicability of the proposed ASC-PWM in systems requiring high-voltage operation or voltage boosting, such as high-voltage DC interfaces or converters operating near the maximum modulation boundary. Nevertheless, for high-power, low-voltage grid-connected rectifier applications, where the DC-link voltage is regulated within an acceptable range, the proposed ASC-PWM is well-suited for achieving improved input power quality, reduced THD, and high power factor.

4.4 Implementation simplicity and computational burden

The proposed ASC–PWM preserves the comparator-based simplicity of conventional carrier-based PWM while improving harmonic performance. In real-time implementation, the computational burden consists of carrier generation, comparison with three modulating signals, and sector-based switching-state selection. Compared with the triangular carrier (linear ramp), the ASC carrier requires one sinusoidal evaluation and one absolute-value operation per switching period, resulting in a slight increase in

computational cost. Compared with SSC–PWM, the additional cost remains comparable, whereas compared with ISC–PWM, the proposed method avoids half-cycle polarity inversion and associated conditional logic, thereby reducing implementation complexity.

From a controller perspective, the proposed method does not require additional sensing variables, predictive algorithms, or online dwell-time recalculation. Its DSP implementation involves standard carrier generation, three comparators, and the existing DSVM sector-identification routine. For FPGA realization, the ASC carrier can be efficiently implemented using a sine lookup table or CORDIC-based generator, followed by a simple absolute-value operation. The switching-table lookup complexity remains unchanged, as the proposed method modifies only the carrier waveform without altering the sector-dependent switching-state mapping.

At this stage of development, the work is limited to analytical and simulation-based validation to isolate the effect of carrier reshaping from hardware-dependent factors, such as parasitics, sensor noise, and gate-driver delays, ensuring a fair comparison among TC-, SSC-, ISC-, and ASC-based DSVM schemes. Although experimental validation is not included, the proposed method is compatible with practical hardware implementation, as it requires no additional power devices or auxiliary circuits beyond conventional DSVM structures. Therefore, the ASC–PWM can be considered hardware-feasible without introducing additional implementation complexity, and this study serves as a method-establishment stage before prototype-level validation.

5. Voltage-Oriented Control Technique

A VOC scheme is employed to regulate the DC-link voltage and enhance the grid-side power quality of the proposed three-phase rectifier. This strategy is commonly adopted in grid-connected converters to suppress DC-link voltage ripple, reduce input current THD, and ensure unity power factor operation. In the VOC technique, the three-phase grid voltages and currents in the stationary abc frame are transformed into a synchronous rotating dq frame aligned with the grid-voltage vector through a phase-locked loop (PLL). Under this alignment, the d-axis is coincident with the grid voltage, yielding $v_{qg} = 0$ and simplifying the instantaneous power expressions. The grid-side active and reactive powers (P_g and Q_g) can be expressed as:

$$P_g = \frac{3}{2} v_{dg} i_{dg}, \; Q_g = -\frac{3}{2} v_{dg} i_{qg} \tag{13}$$

This indicates that the active and reactive powers are independently controlled by the d- and q-axis current components, respectively. Based on this decoupling property, the VOC technique employs three PI controllers, consisting of one outer DC-link voltage controller and two inner current controllers in the synchronous frame. The outer voltage loop regulates the DC-link voltage (v_{dc}) by comparing it with its reference (v_{dc}^*). The resulting voltage error is processed by the first PI controller to generate the reference d-axis current (i_{dg}^*), as expressed below. Furthermore, the voltage-loop gains K_{p1} and K_{i1} are selected based on the DC-link capacitance (C_{dc}), angular frequency (ω_g), and damping factor $\xi = 0.707$ [5].

$$i_{dg}^{\,*} = K_{p1}(v_{dc}^{\,*} - v_{dc}) + K_{i1}\int (v_{dc}^{\,*} - v_{dc})\, d(t) \tag{14}$$

$$K_{p1} \geq C_{dc}\xi\omega_g \quad \text{and} \quad K_{i1} \geq 0.5 C_{dc}\xi\omega_g \tag{15}$$

The inner current loop consists of two synchronous-frame PI controllers. The first current controller regulates the d-axis current by minimizing the error between i_{dg}^* and the measured current i_{dg}, thereby generating the reference converter voltage (v_{dg}^*). The second current controller regulates the q-axis current component to zero in order to enforce reactive-power minimization and power factor correction. Accordingly, the d- and q-axis reference voltages are obtained as:

$$v_{dg}^{\,*} = K_{p2}(i_{dg}^{\,*} - i_{dg}) + K_{i2}\int (i_{dg}^{\,*} - i_{dg})\, d(t) \tag{16}$$

$$v_{qg}^{*} = K_{p2}(-i_{qg}) + K_{i2}\int(-i_{qg})\,d(t) \tag{17}$$

The current-loop gains K_{p2} and K_{i2} are determined from the input parameters as:

$$K_{p2} = \alpha_i L_i \quad \text{and} \quad K_{i2} = \alpha_i R_i \tag{18}$$

where the bandwidth (α_i) is typically limited to one-tenth of the switching frequency to ensure fast response and adequate stability margin. For this technique, the current loop is designed to be significantly faster than the voltage loop to ensure dynamic decoupling. During sector transitions, the DSVM-based modulation maintains continuous switching behavior due to the symmetry of adjacent sectors and the carrier-based implementation, resulting in smooth current tracking without noticeable transients.

6. Results and Discussions

The steady-state performance of the proposed ASC-PWM-based DSVM strategy was evaluated and compared against the conventional TC-PWM, SSC-PWM, and ISC-PWM schemes under identical operating conditions. The key system parameters are summarized in Table 2.

Table 2 Key parameters for the simulated system

Parameters	Symbol	Value
Output power	P_{out}	6 kW
DC-link voltage	V_{dc}	800 V
Grid voltage (RMS)	V_{ag}, V_{bg}, V_{cg}	230 V
Grid frequency	f_g	50 Hz
Switching frequency	f_{sw}	2.5 kHz
Input inductance	L_i	5 mH
Input resistance	R_i	5 Ω
DC-link capacitor	C_{dc}	2200 μF
Voltage controller	K_{p1}	0.244
Voltage controller	K_{i1}	0.122
Current controller	K_{p2}	7.85
Current controller	K_{i2}	7.85×10^3

6.1 Steady-state performance comparison

In Table 3, the term “Not Operable” indicates that the corresponding modulation strategy cannot sustain stable rectifier operation at the specified modulation index. This behavior is attributed to the characteristics of DSVM-derived modulating signals at low modulation indices, where the normalized modulating signals remain close to unity over extended intervals within each fundamental cycle. When compared with the carrier according to Eq. (6), the resulting switching function g_i stays at logic state “1” for a prolonged duration, therefore limiting effective switching transitions.

This effect is more pronounced for sharp-peaked carriers, such as triangular and inverted sine carriers, whose steep slopes near the peak delay comparator crossings and further extend the high switching state. Consequently, the controllable power switches tend to remain in a quasi-permanent ON state, degrading pulse modulation, DC-link regulation, and input-current shaping. Accordingly, stable operation is only achieved above $m_a \approx 0.30$ for the TC-PWM-based DSVM and $m_a \approx 0.60$ for the ISC-PWM-based DSVM.

In contrast, the proposed ASC-PWM-based DSVM provides smoother temporal mapping and maintains sufficient switching transitions even at lower modulation indices, resulting in stable operation over a wider range and lower input-current THD and improved power factor compared with conventional carriers. Although the proposed scheme yields a lower DC-link voltage level (542–1282 V) than the compared methods, this reduction is primarily attributed to the reduced effective duty cycle and nonlinear pulse redistribution introduced by the ASC waveform.

This characteristic reflects its emphasis on harmonic performance and power-factor improvement rather than voltage boosting. Therefore, the proposed ASC-PWM-based DSVM is well suited for high-power, low-voltage grid-connected three-phase two-level rectifier applications, where input power quality is the primary design objective.

Table 3 Steady-state performance comparison of carrier-based DSVM schemes for the Vienna delta-switch rectifier

m_a	Performance indices	TC-PWM	SSC-PWM	ISC-PWM	Proposed ASC-PWM
0.2	Input current THD (%)	Not Operable	20.02	Not Operable	12.63
	DPF (%)		88.23		95.82
	pf (%)		86.51		95.07
	DC-link voltage (V)		2,006		1,282
0.3	Input current THD (%)	21.29	18.62	Not Operable	11.51
	DPF (%)	84.26	94.81		98.23
	pf (%)	82.42	93.21		97.58
	DC-link voltage (V)	1,631	1,520		1,071
0.4	Input current THD (%)	19.55	16.43	Not Operable	11.41
	DPF (%)	94.30	96.70		99.29
	pf (%)	92.55	95.42		98.65
	DC-link voltage (V)	1,518	1,304		958
0.5	Input current THD (%)	18.55	15.29	Not Operable	10.87
	DPF (%)	96.86	98.23		99.56
	pf (%)	95.23	97.10		98.97
	DC-link voltage (V)	1,152	1,142		815
0.6	Input current THD (%)	16.72	14.76	15.79	10.83
	DPF (%)	98.17	98.40	97.86	99.69
	pf (%)	96.83	97.35	96.53	99.11
	DC-link voltage (V)	947	971	1,256	719
0.7	Input current THD (%)	16.58	13.99	16.68	10.00
	DPF (%)	99.05	99.00	95.67	99.80
	pf (%)	97.71	98.05	94.22	99.31
	DC-link voltage (V)	810	872	1,004	670
0.8	Input current THD (%)	16.29	13.85	17.62	10.69
	DPF (%)	99.21	99.25	96.89	99.80
	pf (%)	97.92	98.31	94.79	99.24
	DC-link voltage (V)	703	783	925	620
0.9	Input current THD (%)	16.25	13.62	21.18	11.21
	DPF (%)	99.43	99.33	98.46	99.80
	pf (%)	98.14	98.42	94.86	99.18
	DC-link voltage (V)	620	700	807	566
1.0	Input current THD (%)	15.72	18.31	27.81	11.06
	DPF (%)	99.56	99.40	98.82	99.89
	pf (%)	98.35	97.77	98.82	99.28
	DC-link voltage (V)	563	609	659	542

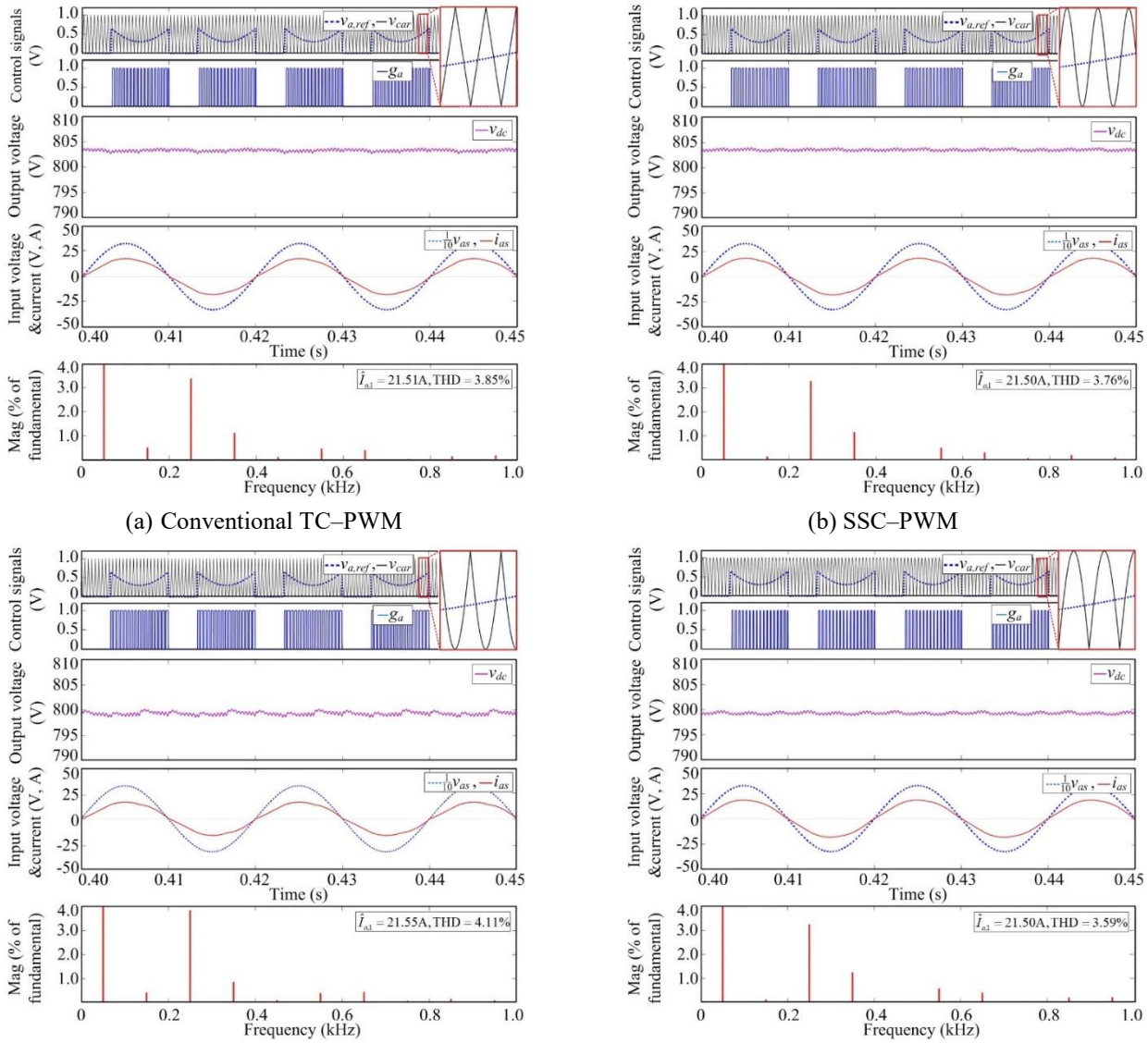
Fig. 4 compares the steady-state performance of the Vienna delta-switch rectifier under VOC-based control for four carrier-based DSVM schemes. The DC-link voltage, input voltage, input phase current waveforms, and harmonic spectra are evaluated under identical conditions.

With the conventional TC-PWM-based DSVM (Fig. 4(a)), uniformly spaced switching pulses are obtained due to the linear carrier slope. The DC-link voltage is regulated at 803 V with 0.38% regulation; however, noticeable current distortion near zero crossings results in clustered harmonics and an input current THD of 3.85%. Using the SSC-PWM-based DSVM (Fig. 4(b)), the nonlinear slope produces a smoother pulse distribution while maintaining comparable DC-link regulation, reducing the input current THD to 3.76%.

In contrast, the ISC–PWM–based DSVM (Fig. 4(c)) concentrates pulses near the switching-period edges. Although the DC-link voltage remains stable (799 V, 0.13%), the edge-centered clustering tends to increase low-order harmonics, resulting in a higher input current THD of 4.11%, consistent with the pulse concentration effect discussed in the modulation analysis.

The proposed ASC-PWM-based DSVM (Fig. 4(d)) redistributes pulses toward the center of each switching interval due to its valley-centered profile. This produces a more uniform input current and shifts dominant harmonics to higher frequencies, achieving the lowest input current THD of 3.59% while maintaining tight DC-link regulation (799 V, 0.13%), comparable to the ISC technique.

In general, all techniques are capable of maintaining the voltage regulation under the VOC control method. However, when considering both harmonic performance and voltage stability, the proposed ASC-PWM-based DSVM scheme exhibits a more favorable trade-off. This advantage is particularly evident in the improved harmonic distribution without increasing switching frequency or computational complexity, making the proposed method well-suited for high-performance Vienna delta-switch rectifier applications requiring improved input power quality.



(a) Conventional TC–PWM (b) SSC–PWM

(c) ISC–PWM (d) Proposed ASC–PWM

Fig. 4 Steady-state performance comparison of four carrier-based DSVM schemes for the Vienna delta-switch rectifier under VOC-based power factor correction control

6.2 Discussion on TSV, cost function, power loss, and efficiency

In addition to harmonic performance, the proposed ASC-PWM-based DSVM can also be evaluated in terms of total standing voltage (TSV), cost function, power loss, and efficiency. TSV is defined as the sum of blocking voltages of all semiconductor devices, while the cost function reflects the overall hardware complexity, including device count and passive components [23].

Since the proposed ASC-PWM modifies only the carrier waveform without changing the converter topology, switching devices, or DC-link structure, both TSV and cost function remain unchanged compared with conventional TC-, SSC-, and ISC-based DSVM schemes. Therefore, no additional voltage stress or hardware cost is introduced, and the proposed method preserves the original hardware configuration of the converter.

In contrast, power loss and efficiency can be influenced indirectly by the modulation strategy, even when the topology is unchanged. The total power loss ($P_{total\ loss}$) can be expressed as the sum of conduction and switching power losses (P_{cl} and P_{sl}).

$$P_{total\ loss} = P_{cl} + P_{sl} \tag{19}$$

Also, the corresponding efficiency (η) is:

$$\eta = \frac{P_{out}}{P_{out} + P_{total\ loss}} \tag{20}$$

Although the switching frequency is identical for all methods, the proposed ASC-PWM improves current waveform quality, resulting in lower THD and higher power factor, as shown in Table 3. This may lead to a reduction in RMS current and associated conduction losses, thereby potentially improving overall efficiency. Furthermore, recent studies highlight that modern power electronic converters should be evaluated not only in terms of voltage utilization but also efficiency and system-level integration capability, particularly in advanced energy systems and high-power applications [24]. In this case, the proposed method improves power quality and efficiency at the control level without raising the cost of TSV or hardware. This presents a favorable trade-off for real-world rectifier applications.

7. Conclusion

This paper presented a novel ASC-PWM-based DSVM strategy for the Vienna delta-switch rectifier. The proposed approach employs an analytically defined ASC within a conventional comparator-based PWM structure to reshape switching-pulse distribution without increasing switching frequency or computational complexity. Sector-dependent switching-state remapping and nearest-three-vector DSVM modulating signals were derived to satisfy the rectifier's unidirectional current-flow constraint and ensure compatibility with the topology. The modulation stage was integrated with a VOC-based power factor correction controller to achieve DC-link voltage regulation and improved grid-side power quality. The principal findings are summarized as follows:

(1) The ASC-PWM-based DSVM can provide stable switching operation over a wider modulation index range compared with TC-PWM and ISC-PWM, which exhibit limited operability at low modulation indices.

(2) In the operable region, valley-center pulse redistribution contributes to lower input-current THD and higher power factor for the proposed method.

(3) The proposed method consistently produces a lower DC-link voltage than conventional carrier-based approaches, which is primarily attributed to the reduced effective duty cycle introduced by the ASC waveform.

(4) With VOC-controlled operation, the minimum input-current THD is obtained as 3.59%, and its tight DC-link voltage regulation (≈799 V, 0.13%) is still maintained by the proposed scheme.

(5) The proposed ASC carrier modulation enhances harmonic spreading without increasing switching frequency or algorithmic complexity, while maintaining the simplicity of comparator-based PWM implementation.

Overall, the proposed ASC-PWM-based DSVM provides a lower DC-link voltage than conventional carrier-based methods, due to the reduced effective duty cycle caused by nonlinear carrier shaping. Despite this reduction, the method achieves superior harmonic performance, lower THD, and high power factor, making it suitable for high-power, low-voltage grid-connected

applications of Vienna rectifiers with stringent input power quality requirements. Future work will focus on experimental validation to further verify the proposed ASC-PWM strategy under practical operating conditions.

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Conflicts of Interest

The authors declare no conflict of interest.

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