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Resonant-Frequency Tracking Method for Medium-Frequency Inverters Based on RLS and DSOGI-PLL Methods

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Abstract

This study aims to improve resonant-frequency tracking in medium-frequency inverters subjected to switching harmonics and load-parameter variations. The proposed method combines recursive least squares (RLS) feedforward estimation with dual second-order generalized integrator phase-locked loop (DSOGI-PLL) feedback. The RLS algorithm identifies the equivalent resistance and inductance online and calculates the resonant-frequency feedforward value from the estimated inductance. In parallel, two SOGIs extract the fundamental components of the total voltage of the resistor-inductor-capacitor (RLC) circuit and the resonant current, and a normalized cross-product phase detector generates the feedback correction. The method reduces frequency drift after a phase-shift step by approximately 93% and shortens the convergence time after an inductance step from 9.29 ms to 2.32 ms. These results demonstrate that the proposed method can improve resonant-frequency tracking accuracy and dynamic response under phase-shift modulation and load-parameter variations.

Keywords: medium-frequency inverter, resonant-frequency tracking, parameter identification, feedforward compensation

1. Introduction

Medium-frequency inverters are widely used in induction heating, metal melting, and welding preheating. Their efficiency and the soft-switching performance of the semiconductor devices are closely related to impedance matching with the resonant load [1]. Changes in workpiece temperature, magnetic permeability, coil coupling, and load position can alter the equivalent resistance, inductance, and resonant frequency, causing the inverter to deviate from its intended operating point [2]. Online load-parameter estimation and resonant-frequency tracking are therefore essential for adapting medium-frequency inverters to impedance variations, reducing reactive circulation and switching losses, and maintaining soft-switching operation.

For online estimation of induction-heating load parameters, Sarnago et al. [3] implemented resonant-load identification on a field-programmable gate array (FPGA) to enable real-time parameter estimation in flexible induction-heating equipment. Their subsequent work [4] proposed a general resonant-tank identification method to accommodate different induction-heating loads. Li et al. [5] estimated the load from the natural resonant current of a series RLC circuit, thereby reducing the need for additional measurements. Roinila and Khodamoradi [6] further investigated online parameter estimation for quasi-resonant induction-heating inverters. Huang et al. [7] reported a current-sensorless online load-estimation method, reducing the complexity of the sampling chain. Moreover, Zuo and Duan [8] used RLS-based load identification for direct-current (DC) power control of a medium-frequency induction-heating power supply, demonstrating that online parameter estimates can

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provide a basis for operating-point control. These studies establish that inverter voltage and current measurements can be used to obtain load parameters. However, they have mainly focused on parameter estimation or load-state identification, and the coordination between parameter estimates and the frequency-feedback loop has not been sufficiently addressed.

For resonant-frequency tracking, Vishnuram et al. [9] applied a phase-locked loop to power regulation in a dual-half-bridge series-resonant induction-heating inverter to suppress the influence of asymmetric voltage components. Ozbay et al. [10] introduced sliding-mode control into a phase-locked loop (PLL) combined with pulse-density modulation (PDM) to improve dynamic tracking under load variations. To accommodate load changes caused by vessels made of different materials, Jeong et al. [11] proposed an enhanced load-adaptive modulation method for series-resonant inverters. Many existing methods regulate the operating frequency according to the voltage-current phase relationship, but their phase-detector signals are often constructed directly from zero-crossing instants, switching edges, or sign information in the original switching waveforms.

When phase-shift power regulation is applied to a full-bridge inverter, zero-voltage intervals appear in the output voltage, and both the switching-edge positions and harmonic content vary with the phase-shift angle. The zero-crossing events of the original voltage therefore no longer uniquely represent its fundamental phase. If zero-crossing or sign-based phase detection is still applied to the original waveform, the locking point may drift with the phase-shift angle, leading to a steady-state frequency-tracking error.

Xu et al. [12] reviewed SOGI-PLL methods for single-phase synchronization and fundamental extraction under distorted grid conditions. Zhang et al. [13] improved the SOGI-PLL structure to enhance synchronization under non-ideal conditions involving DC offsets and frequency variations. Bamigbade and Khadkikar [14] showed that the orthogonal-component generation structure directly affects phase-detection performance. Stojic et al. [15] improved a fixed-frequency SOGI-PLL for digital-controller implementation, whereas Ahmed [16] developed a SOGI-PLL for rapid frequency-ramp tracking. Furthermore, Mondal et al. [17] combined frequency-adaptive filtering with a SOGI to improve PLL dynamics under disturbances. Recent work has extended SOGI-PLL-based synchronization to resonant power-transfer and single-phase inverter systems. Wang et al. [18] developed a fixed-frequency SOGI-PLL for phase synchronization in a multisegment wireless power transfer system, while Bamigbade et al. [19] proposed an H-infinity robust SOGI-PLL for grid synchronization of single-phase inverters. Collectively, these studies demonstrate that SOGI-PLL structures can improve fundamental-phase estimation under non-ideal waveforms. Their applications, however, have mainly focused on grid synchronization, wireless power transfer, or general single-phase inverter systems.

Taken together, the specific problem addressed here has two aspects. First, phase-shift modulation changes the zero-voltage intervals, switching-edge positions, and harmonic content of the output voltage, so zero-crossing or sign-based detection of the original waveform can shift the PLL locking point. Second, load-parameter changes can slow frequency capture when only feedback correction is used, because the tracker must converge toward the new resonant point.

To address these issues, this paper proposes a resonant-frequency tracking method for series-resonant power supplies that combines RLS feedforward estimation with DSOGI-PLL feedback. The RLS algorithm identifies the equivalent resistance and inductance online, and the estimated inductance is used to calculate a resonant-frequency feedforward value. The DSOGI extracts the in-phase and quadrature fundamental components of the total RLC voltage and resonant current. A normalized cross-product phase detector then makes the feedback correction depend on the fundamental phase relationship rather than on switching-waveform edges. This coordinated design enables rapid frequency adjustment after load-parameter changes while maintaining accurate phase tracking in the presence of phase-shift-induced waveform distortion. The remainder of this paper is organized as follows. Section 2 establishes the inverter and load-identification models. Section 3 presents the proposed DSOGI-PLL and RLS feedforward tracking algorithm. Section 4 reports the simulation and hardware validation results, and Section 5 summarizes the conclusions.

2. System Modelling

The inverter considered in this study is a single-phase full-bridge inverter followed by a series-resonant circuit, as shown in Fig. 1. Here, R and L denote the equivalent resistance and inductance of the heating coil and workpiece, respectively, and$C$denotes the resonant compensation capacitance.

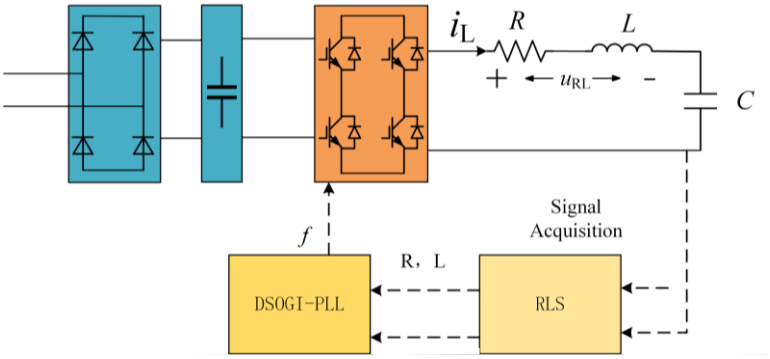


Fig. 1 Topology of the medium-frequency inverter

The resonant frequency of the series-resonant circuit is $f_0 = 1/2\pi\sqrt{LC}$. At resonance, the series-resonant circuit is purely resistive, and the fundamental components of the total RLC voltage and the circuit current are in phase.

2.1 Phase-shift modulation and its influence on the PLL

To achieve a wide power-regulation range, the full-bridge inverter adopts phase-shift modulation. Let ω_s denote the switching angular frequency, $\theta = \omega_s t$ the electrical angle, and β the phase-shift parameter between the two bridge legs, with $0 \le \beta \le \pi$. In this paper, $\beta = 0$ corresponds to the maximum output-pulse width. As β increases, the zero-voltage interval of the output voltage widens, while the effective voltage-pulse width decreases.

Due to the half-wave symmetry of the waveform, its DC component and even-order harmonics are zero. Its Fourier series can be written as:

$$v_{\text{inv}}(t) = \sum_{n=1,3,5..}^{\infty} \frac{4V_{\text{dc}}}{n\pi} \cos\left(n\frac{\beta}{2}\right) \sin(n\omega_{\text{sw}} t) \tag{1}$$

The amplitude ratio of the nth odd-order harmonic to the fundamental component is:

$$\frac{U_{nm}}{U_{1m}} = \left| \frac{\cos(n\beta/2)}{n\cos(\beta/2)} \right| \tag{2}$$

Eq. (2) shows that the phase-shift angle changes not only the fundamental-voltage amplitude but also the relative amplitude of each harmonic. As the effective pulse width decreases, switching edges, zero-voltage intervals, and high-frequency disturbances become more influential relative to the original voltage waveform.

When the operating frequency approaches the series-resonant frequency ($\varphi_1 \approx 0$), the fundamental components of the total RLC voltage and circuit current are approximately in phase. Under ideal symmetric phase-shift modulation, changing β mainly affects the fundamental amplitude and harmonic content, without directly altering the fundamental impedance angle of a given resonant circuit ω_s.

The conventional sign-based phase-locked loop (Sign-PLL) directly compares the zero-crossing instants of the original switching voltage and current. Let the fundamental current be represented as:

$$i_1(\theta) = I_{1m} \sin(\theta - \varphi_1) \tag{3}$$

Its rising zero-crossing instant is $\theta_{i,zc} = \varphi_1$. However, a zero-voltage interval with a width of β exists around the theoretical zero crossing of the fundamental component in the phase-shifted voltage, so the original voltage lacks a unique zero-crossing instant. If the zero-crossing detector defines the transition from the zero-voltage interval to the positive-voltage level as the rising zero-crossing event, then $\theta_{u,zc} = \beta/2$. The phase error obtained by the conventional zero-crossing phase detector is therefore defined as:

$$e_{zc} = \theta_{i,zc} - \theta_{u,zc} = \varphi_1 - \frac{\beta}{2}. \tag{4}$$

If the PLL uses $e_{zc} = 0$ as its locking condition, its steady-state equilibrium point becomes $\varphi_1 = \beta/2$. This differs from the condition $\varphi_1 = 0$ required for series resonance. Consequently, a change in the phase-shift angle moves the equilibrium point of the conventional zero-crossing phase detector and appears as a frequency-tracking error. If the detector selects the opposite edge of the zero-voltage interval, the direction of the error is reversed. Considering dead time, switching spikes, sampling delay, and the hysteresis threshold, the practical phase error can be summarized as:

$$e_{zc} = \varphi_1 \pm \frac{\beta}{2} + \Delta\varphi_d \tag{5}$$

Here, $\Delta\varphi_d$ represents the additional phase error introduced by non-ideal switching processes and the sampling chain.

The DSOGI units extract the in-phase and quadrature fundamental components of the total RLC voltage and circuit current. After amplitude normalization, the phase detector depends on the fundamental phase difference rather than on switching-waveform edges.

2.2 Load-parameter identification model

The RLS inputs are the voltage across the series branch and the circuit current. The continuous-time state equation of the load is given by:

$$u_{RL}(t) = Ri_L(t) + L\frac{di}{dt} \Rightarrow \frac{di_L}{dt} = -\frac{R}{L}i(t) + \frac{1}{L}u_{RL}(t) \tag{6}$$

During each identification interval, u_{RL} is assumed to remain constant. Exact zero-order-hold discretization then gives the discrete-time state equation:

$$i(k) = a \cdot i_L(k-1) + b \cdot u_{RL}(k-1) \tag{7}$$

Here, $a = exp(-RT_s/L)$, and $b = (1-a)/R$, where T_s denotes the actual RLS update period.

The discrete model can be written in the linear regression form: $i(k) = \varphi^T(k)\,\theta(k)$, where the regression vector and parameter vector to be identified are, respectively:

$$\varphi(k) = \begin{bmatrix} i(k-1) \\ u_{RL}(k-1) \end{bmatrix}, \ \theta(k) = \begin{bmatrix} a(k) \\ b(k) \end{bmatrix} \tag{8}$$

The discrete parameters are estimated online from the sampled resistive-inductive (RL) branch voltage and circuit current, after which the equivalent resistance and inductance are recovered. Subsequently, the identified inductance is used to calculate the resonant-frequency feedforward value.

3. Resonant-Frequency Tracking Algorithm

The DSOGI-PLL takes the total RLC voltage and resonant current at the inverter output as inputs. Two SOGIs extract their in-phase and quadrature fundamental components, from which a frequency-feedback correction is generated according

to the fundamental phase relationship. The RLS algorithm takes the RL-branch voltage and resonant current as inputs to identify the equivalent load parameters online. The two voltage-measurement channels are used for PLL fundamental-phase detection and RLS parameter identification, respectively. The identified inductance is used to calculate the resonant-frequency feedforward value. The proposed composite frequency-tracking structure is shown in Fig. 2.

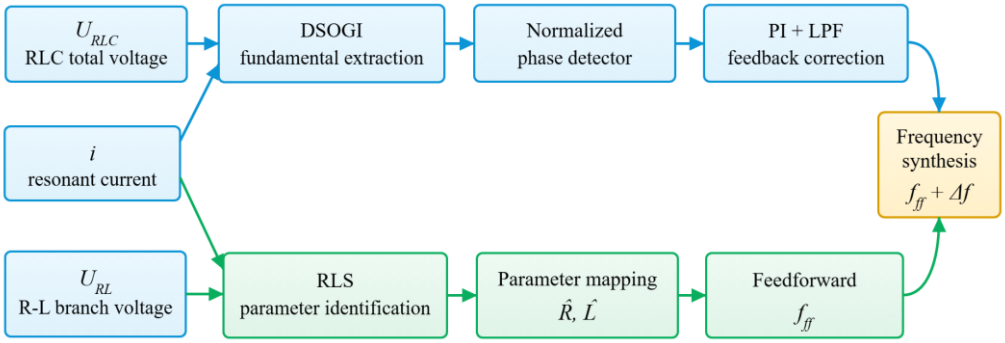


Fig. 2 Structure of the RLS-feedforward and DSOGI-PLL frequency-tracking method

3.1 DSOGI-based fundamental extraction

The second-order generalized integrator (SOGI) is the core element for frequency-adaptive band-pass filtering. Its continuous-time transfer functions are:

$$\begin{cases} D(s) = \dfrac{v_\alpha(s)}{v(s)} = \dfrac{k\omega_0 s}{s^2 + k\omega_0 s + \omega_0^2} \\ Q(s) = \dfrac{v_\beta(s)}{v(s)} = \dfrac{k\omega_0^2}{s^2 + k\omega_0 s + \omega_0^2} \end{cases} \tag{9}$$

Here, v is the input signal, v_α is the in-phase output component, v_β is the quadrature output component lagging the input fundamental by 90°, k is the gain coefficient, and ω_0 is the center angular frequency. $D(s)$ exhibits band-pass-filter characteristics, with unity gain and zero phase at the center frequency, whereas $Q(s)$ has low-pass-filter characteristics and suppresses high-order harmonics. The value of k determines the filtering bandwidth. Considering the trade-off between filtering and dynamic response, $k = \sqrt{2}$ is used.

The SOGI center frequency follows the PLL-estimated frequency, enabling frequency-adaptive fundamental extraction. The continuous-time state equations are discretized using the forward Euler method as follows:

$$x_1(k+1) = x_1(k) + T_s \cdot \omega_0 [k\left(v(k) - x_1(k)\right) - \omega_0 x_2(k)] \tag{10}$$

$$x_2(k+1) = x_2(k) + T_s \cdot x_1(k) \tag{11}$$

The outputs are:

$$v_\alpha = x_1, \quad v_\beta = \omega_0 x_2 \tag{12}$$

3.2 DSOGI-PLL frequency feedback

The DSOGI-PLL takes the total voltage of the series-resonant circuit and the circuit current as inputs. Two SOGIs separately extract the in-phase and quadrature fundamental components of the voltage and current:

$$u_{dq} = \begin{bmatrix} u_\alpha & u_\beta \end{bmatrix}^{\mathrm{T}}, \; i_{dq} = \begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^{\mathrm{T}} \tag{13}$$

To reduce the influence of the fundamental-amplitude variations caused by phase-shift modulation on the phase-detector gain, the two sets of quadrature components are normalized as follows:

$$\begin{cases} U_{\mathrm{m}} = \sqrt{u_\alpha^2 + u_\beta^2 + \varepsilon}\ ,\ I_{\mathrm{m}} = \sqrt{i_\alpha^2 + i_\beta^2 + \varepsilon} \\ u_{\alpha n} = u_\alpha / U_{\mathrm{m}}\ ,\ u_{\beta n} = u_\beta / U_{\mathrm{m}} \\ i_{\alpha n} = i_\alpha / I_{\mathrm{m}}\ ,\ i_{\beta n} = i_\beta / I_{\mathrm{m}} \end{cases} \tag{14}$$

Here, ε is a small positive constant introduced to prevent division by zero at low signal amplitudes.

The cross-product phase-detector signal is constructed from the normalized quadrature components by:

$$e_\phi(k) = u_{\alpha n}(k) i_{\beta n}(k) - u_{\beta n}(k) i_{\alpha n}(k) \tag{15}$$

Let the voltage and current phases be θ_u and θ_i, respectively. Then:

$$e_\phi(k) = \sin\left[\theta_u(k) - \theta_i(k)\right] \tag{16}$$

Thus, at resonance, the voltage and current fundamentals are in phase, satisfying $\theta_u - \theta_i = 0$ and $e_\phi = 0$. The sign of the phase-detector signal indicates whether the operating frequency should be increased or decreased to maintain tracking.

A first-order low-pass filter is employed to suppress high-frequency disturbances in the phase-detector signal:

$$\bar{e}_\phi(k) = (1-\alpha)\bar{e}_\phi(k-1) + \alpha e_\phi(k) \tag{17}$$

Here, $\alpha = 2\pi f_{\mathrm{LPF}} T_s$ is the corresponding discrete-time coefficient, f_{LPF} is the phase-error filter bandwidth, and T_s is the control period.

The PI frequency corrector then generates a frequency correction from the filtered phase error:

$$\begin{cases} \xi(k) = \xi(k-1) - K_i T_s \bar{e}_\phi(k) \\ \Delta f_{\mathrm{PLL}}(k) = -K_p \bar{e}_\phi(k) + \xi(k) \end{cases} \tag{18}$$

The negative-feedback correction drives the fundamental phase error toward zero.

For the DSOGI-PLL without RLS feedforward, the frequency command f_{init} is used as the reference for frequency adjustment, which is given by:

$$f_{\mathrm{cmd}}^{\mathrm{DSOGI}}(k) = \mathrm{sat}\left[f_{\mathrm{init}} + \Delta f_{\mathrm{PLL}}(k) \right] \tag{19}$$

Here, the SOGI center angular frequency is updated synchronously with the final frequency command as $sat\,(x) = min[f_{max}, max(f_{min}, x)]$, and the corresponding discrete update is $\omega_{\mathrm{SOGI}}(k) = 2\pi f_{\mathrm{cmd}}(k)$. Thus, the DSOGI center frequency, PLL-estimated frequency, and inverter switching frequency remain synchronized, allowing the frequency-tracking loop to continuously correct the operating frequency according to the fundamental phase error.

3.3 RLS and DSOGI-PLL frequency-tracking method

3.3.1 Variable-forgetting-factor RLS recursion

Based on the discrete load model established in Section 2.2, the RLS algorithm estimates the parameter vector online. Using the parameter estimate from the previous instant, the predicted current and prediction error are, respectively:

$$\begin{cases} \hat{i}(k) = \varphi^{\mathrm{T}}(k)\ \theta(k-1) \\ \varepsilon(k) = i(k) - \hat{i}(k) \end{cases} \tag{20}$$

To balance the tracking speed during load-parameter changes with steady-state identification accuracy, a variable forgetting factor related to the prediction error is introduced:

$$\lambda(k)=\lambda_{\min}+(1-\lambda_{\min})\exp\left[-\gamma\varepsilon^{2}(k)\right] \tag{21}$$

Here, $\lambda_{\min}$ is the lower bound of the forgetting factor and γ represents the error-sensitivity coefficient. When the prediction error is large, $\lambda(k)$ decreases, reducing the weight of historical data and accelerating parameter adaptation. As the prediction error decreases, $\lambda_{\min}$ gradually approaches 1, and the resulting update is given by $\lambda(k)$, thereby reducing steady-state parameter fluctuations.

The recursion of the variable-forgetting-factor RLS algorithm is expressed as:

$$\begin{cases} K(k)=\dfrac{P(k-1)\varphi(k)}{\lambda(k)+\varphi^{\mathrm{T}}(k)P(k-1)\varphi(k)} \\ \theta(k)=\theta(k-1)+K(k)\boldsymbol{\varepsilon}(k) \\ P(k)=\dfrac{1}{\lambda(k)}\left[I-K(k)\varphi^{\mathrm{T}}(k)\right]P(k-1) \end{cases} \tag{22}$$

Here, $K(k)$ is the gain matrix, $P(k)$ is the covariance matrix, and $\hat{\theta}(k)$ is the parameter estimate at the kth update instant. The recursive result yields $\hat{a}(k)=\hat{\theta}_1(k)$, and $\hat{b}(k)=\hat{\theta}_2(k)$.

The equivalent resistance and inductance are then recovered from the parameter-mapping relationships in Section 2.2. The identified inductance is used to construct the resonant-frequency feedforward value.

3.3.2 Resonant-frequency feedforward and feedback correction

The RLS-identified inductance is used to calculate a feedforward resonant frequency, reducing the search required by feedback alone after a load change. According to the series-resonance condition, the resonant frequency is calculated from the identified inductance as follows:

$$f_{ff}=\frac{1}{2\pi\sqrt{\hat{L}\cdot C}} \tag{23}$$

In the proposed feedforward-feedback frequency-tracking structure, the RLS-calculated feedforward frequency replaces the fixed initial frequency used by the standalone DSOGI-PLL, and the frequency correction generated by the DSOGI-PLL is then applied. The final frequency command is:

$$f_{\mathrm{cmd}}^{\mathrm{RLS+DSOGI}}(k)=\mathrm{sat}\left[f_{\mathrm{ff}}(k)+\Delta f_{\mathrm{PLL}}(k)\right] \tag{24}$$

4. Simulation and Hardware Experimental Validation

4.1 Simulation validation

To verify the effectiveness of the proposed method, a series-resonant induction-heating power supply and its frequency-tracking model were developed in MATLAB/Simulink. The frequency trajectories and steady-state locking frequencies of different methods were examined, together with online parameter identification and frequency-tracking tests. The main simulation parameters are listed in Table 1.

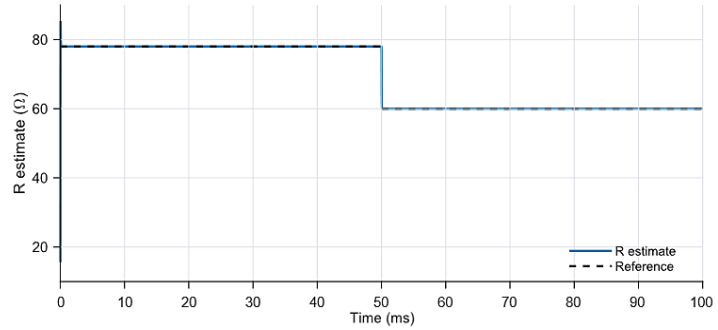
Table 1 Main simulation parameters

Parameter	Value
DC-link voltage / V	311
Resonant capacitance / nF	16.9
Initial equivalent inductance / mH	4.04
Initial equivalent resistance / Ω	78
Initial operating frequency / kHz	20
Sampling time / s	1×10^{-7}

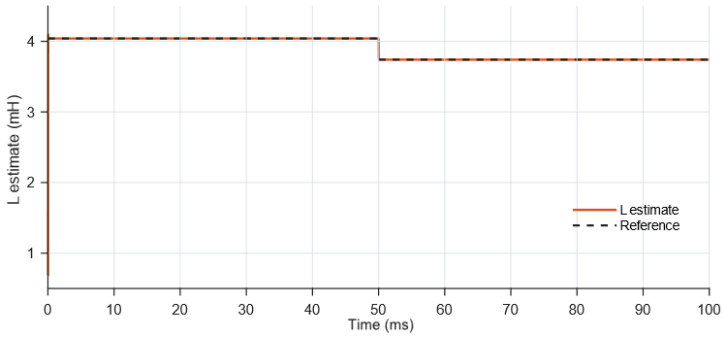
The simulation used $K_p = 1400$ and $K_i = 9.0 \times 10^5$. The phase-detector and phase-output low-pass filters had bandwidths of 500 Hz and 100 Hz, respectively. The regularization constant in the amplitude normalization was set to $\varepsilon = 1.0 \times 10^{-6}$. The DSOGI-PLL frequency was limited to 15–25 kHz. The simulation sampling period was $T_s = 0.1\mu s$, and the RLS recursion was executed once per simulation step; therefore, the RLS update period was also 0.1 μs. The lower bound of the forgetting factor was set to $\lambda_{min} = 0.98$ and the error-sensitivity coefficient was $\gamma = 5 \times 10^7$.

For the transient comparisons, the steady-state frequency was defined as the mean value over the final 5 ms of each response. The frequency-convergence time was defined as the first timestamp at which the absolute frequency error entered the specified tolerance band and remained within it for at least 1 ms. A ±10 Hz band was used for the simulation and a ±30 Hz band for the hardware experiment. The phase-convergence time was defined similarly using a ±1° phase-error band and the same 1-ms holding interval. For the RLS parameter-identification results, the settling time was defined separately as the first timestamp at which the relative estimation error entered the corresponding tolerance band and remained within it for at least 1 ms, with ±1% for simulation and ±2% for hardware experiments. In all cases, the reported time corresponds to the beginning of the qualifying interval.

The effectiveness of the RLS-based parameter identification was first verified under different load conditions. Two representative cases were considered, and the tracking performance of the estimated resistance and inductance was analyzed. The simulation results are shown in Fig. 3.



(a) Resistance estimate

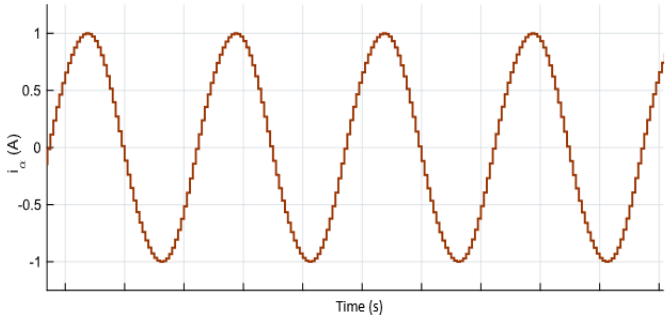


(b) Inductance estimate

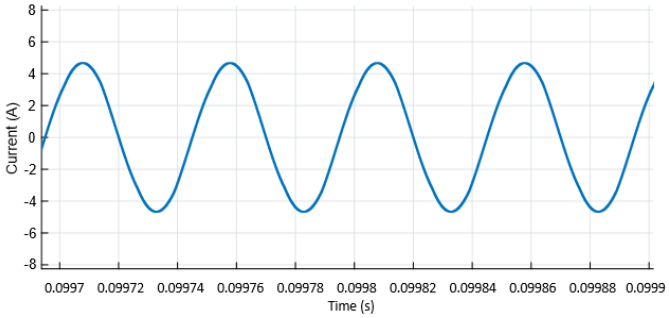
Fig. 3 Online load-parameter identification results

The RLS algorithm accurately identified the equivalent resistance and inductance under the two representative load conditions. The maximum relative errors were 0.045% for the resistance estimate and 0.006% for the inductance estimate. The estimates entered the corresponding ±1% parameter-error bands within approximately 0.1 ms and remained within these bands thereafter. These small identification errors provide sufficiently accurate inductance information for the subsequent resonant-frequency feedforward calculation.

To verify the fundamental-extraction capability of the DSOGI under phase-shift modulation, the inverter output voltage containing a zero-voltage freewheeling interval and the resonant current were used as inputs. The in-phase and quadrature components generated by the SOGI were then examined.

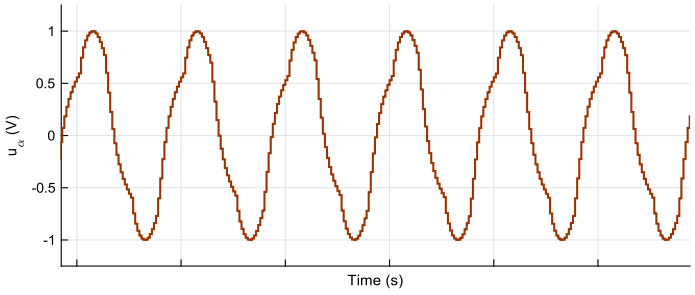


(a) Fundamental component

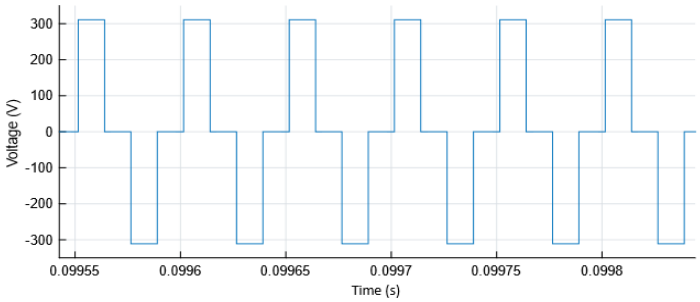


(b) Original current

Fig. 4 Comparison between the fundamental and original current waveforms



(a) Fundamental component

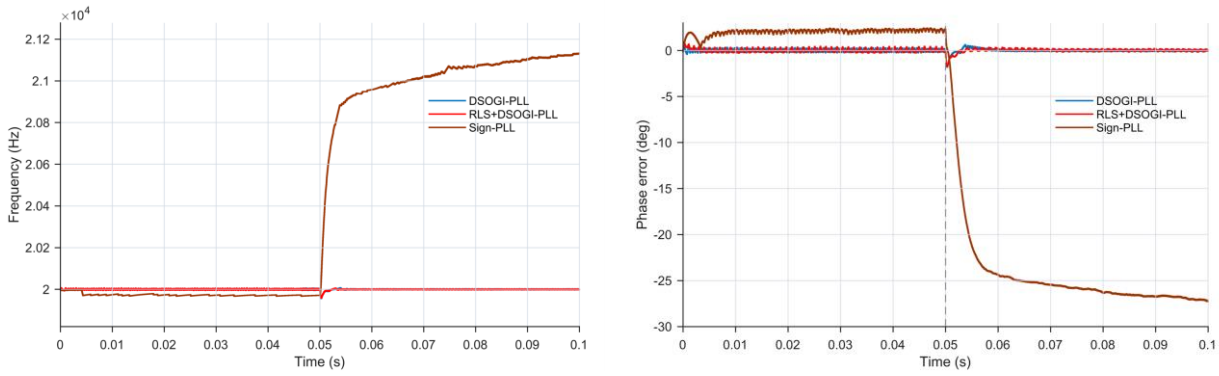


(b) Original voltage

Fig. 5 Comparison between the fundamental and original voltage waveforms

As shown in Figs. 4 and 5, the original output voltage contains clear switching harmonics and zero-voltage intervals, whereas the voltage fundamental extracted by the DSOGI is approximately sinusoidal. The phase relationship between the current fundamental and its quadrature component is also stable. These results indicate that the DSOGI effectively suppresses the high-order harmonics introduced by phase-shift modulation and provides cleaner phase information for the normalized cross-product phase detector.

To evaluate the influence of phase-shift modulation on the conventional PLL, the load parameters were kept constant while the full-bridge phase-shift angle was changed. The frequency-tracking responses of the conventional Sign-PLL, DSOGI-PLL, and RLS+DSOGI-PLL were compared. In the simulation, the phase-shift angle was stepped between different power levels, and the frequency responses of the three methods were recorded.

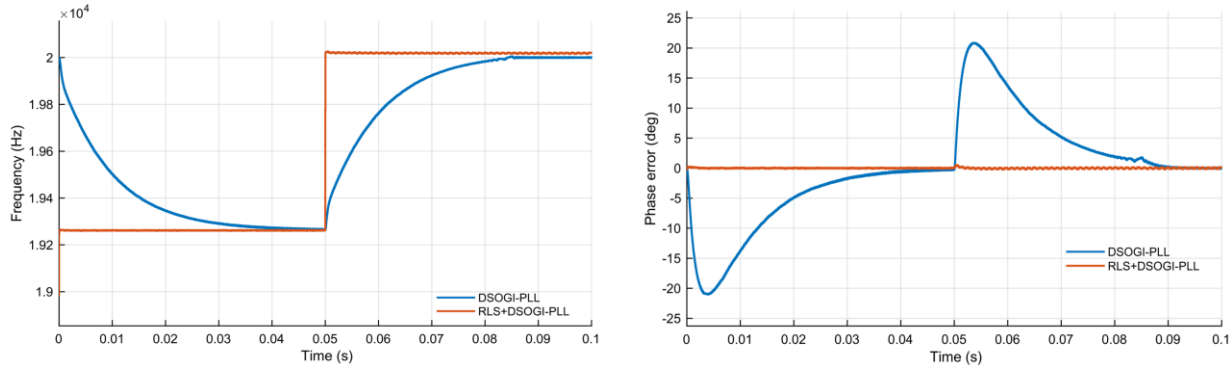


(a) Frequency-tracking response (b) Corresponding phase-error response

Fig. 6 Comparison of frequency and phase-error responses to a phase-shift step

As shown in Fig. 6, the phase-shift step causes a clear displacement of the Sign-PLL equilibrium point, and its output frequency increases from 19,964 Hz to 21,186 Hz. The phase errors of the DSOGI-PLL and RLS+DSOGI-PLL briefly fluctuate and then converge toward zero, with steady-state frequencies of 20,015 Hz and 20,019 Hz, respectively. These results show that DSOGI-based fundamental extraction and normalized phase detection reduce the influence of the phase-shift-induced zero-voltage interval on the locking point.

To verify the frequency-tracking performance of the proposed method under a load-parameter step change, the load inductance was changed during operation. The frequency-convergence curves and phase-error responses of the DSOGI-PLL and RLS+DSOGI-PLL were compared.



(a) Frequency-convergence comparison (b) Corresponding phase-error comparison

Fig. 7 Comparison of frequency and phase-error responses under an inductance step change

As shown in Fig. 7, after the inductance change, the DSOGI-PLL adjusts the operating frequency according to the fundamental phase error. Its maximum phase error is 20.80°, and its frequency-convergence time is 32.98 ms. By contrast, the RLS+DSOGI-PLL uses the identified inductance to calculate a resonant-frequency feedforward value, first positioning the operating frequency near the new resonant point and then applying a small DSOGI-PLL feedback correction. Its maximum phase error decreases to 2.91°, and its frequency-convergence time is reduced to 2.54 ms. This representative case shows that RLS feedforward shortens frequency capture and reduces the transient phase deviation after a load step.

4.2 Hardware experimental validation

A simulation model may not fully capture sampling delay, sensor noise, and switching spikes in a practical system, all of which can affect load-parameter identification and fundamental phase detection. Therefore, the proposed frequency-tracking method was further validated on a 500 W medium-frequency inverter prototype. The nominal load parameters were R = 5 Ω, L = 144 μH, and C = 0.47 μF, and the operating frequency was approximately 20 kHz. The controller was implemented on a TMS320F280049C platform. The ADC sampling frequency was 2 MHz, corresponding to a 0.5 μs sample interval. The data were processed in 512-sample DMA frames, giving a frame-processing period of 256 μs. Within each frame, the DSOGI and

RLS recursions were performed at every sample using a 0.5 μs sampling interval. In this implementation, the PWM switching frequency was generated from the final frequency command of the frequency-tracking controller rather than from a separate fixed control frequency. The bridge switching-frequency command was limited to 10–35 kHz, while the closed-loop operating range was constrained to 19–22 kHz. The reference resistance and inductance values were measured independently using an LCR meter. The prototype is shown in Fig. 8.

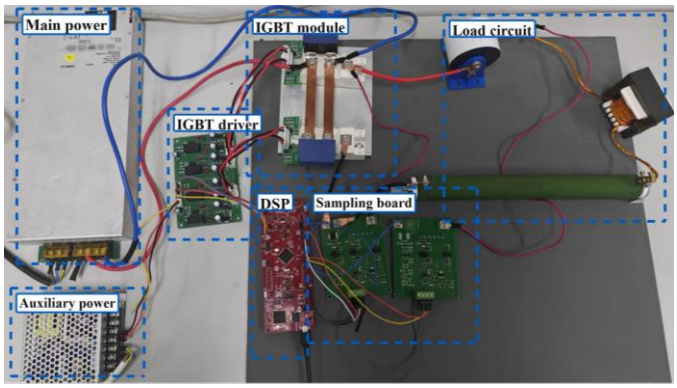
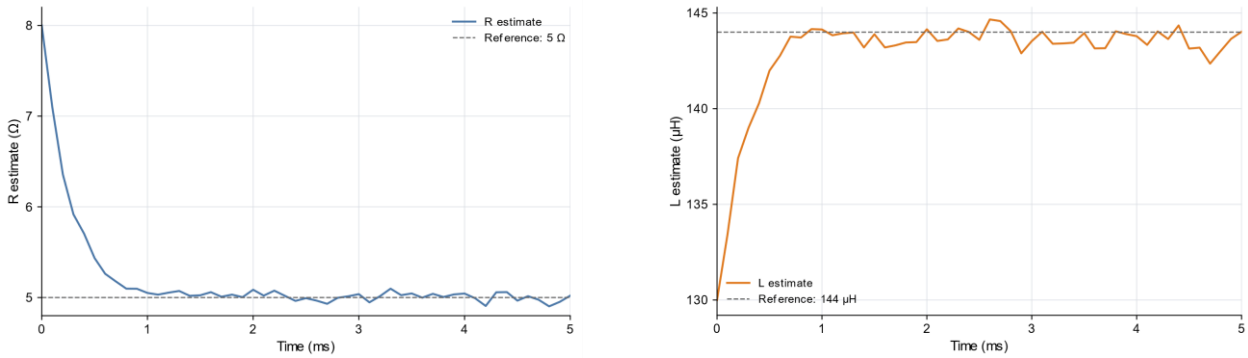


Fig. 8 Photograph of the experimental prototype

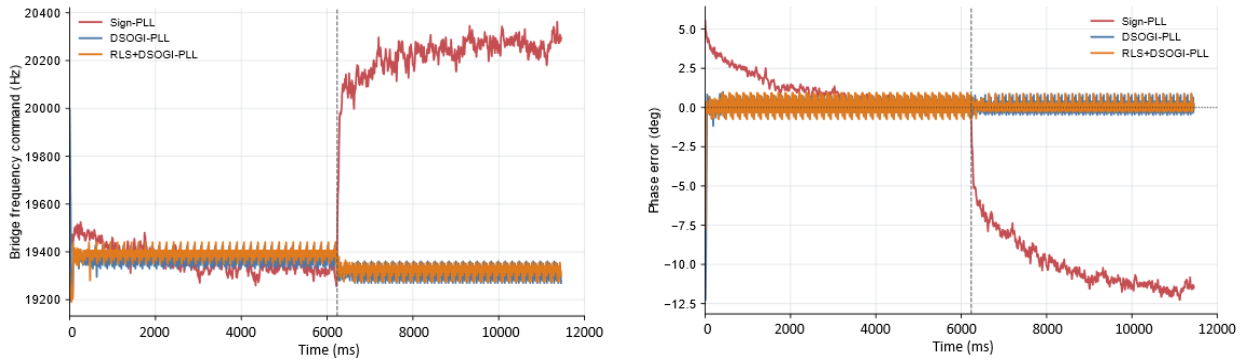
The online parameter-identification performance of the hardware-implemented RLS algorithm was evaluated using the results shown in Fig. 9. After the RLS algorithm was enabled, both estimates gradually converged toward their reference values. The inductance estimate entered the ±2% parameter-error band at approximately 0.5 ms, while the resistance estimate entered the same band at approximately 0.8 ms. After both estimates had entered and remained within the ±2% parameter-error band, the maximum steady-state relative errors over the remaining recorded interval were 1.96% for resistance and 1.14% for inductance, respectively. These results indicate that the discrete identification model can estimate the load parameters with reasonable accuracy under practical sampling noise and switching interference.



(a) Resistance estimate (b) Inductance estimate

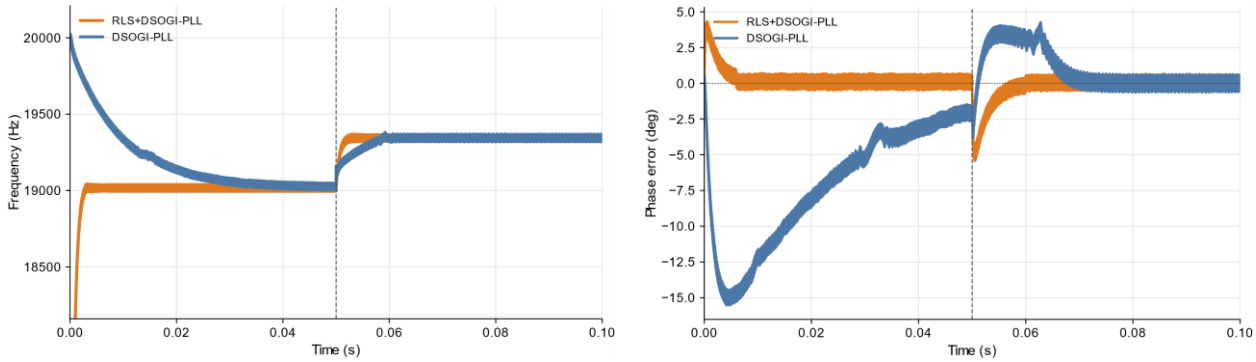
Fig. 9 Hardware results of RL parameter identification

To evaluate the influence of phase-shift modulation on different frequency-tracking methods, the load parameters were kept constant, and the phase-shift angle was stepped to 60°. The corresponding frequency and phase-error responses are shown in Fig. 10(a) and (b), respectively. Before and after the phase-shift change, the steady-state frequency of the Sign-PLL drifted from approximately 19,320.2 Hz to 20,296.7 Hz, corresponding to a frequency shift of 976.5 Hz. This result shows that changes in the zero-voltage interval and switching-edge positions of the original switching voltage can shift the equilibrium point of the conventional zero-crossing phase detector. By comparison, the steady-state frequency changes of the DSOGI-PLL and RLS+DSOGI-PLL were approximately 62.0 Hz and 67.0 Hz, respectively, corresponding to reductions of approximately 93.7% and 93.1% relative to the Sign-PLL drift. The two DSOGI-based methods maintained similar steady-state frequencies after the phase-shift change, indicating that fundamental extraction and normalized phase detection effectively reduce the influence of zero-voltage intervals and switching harmonics on the frequency locking point.



(a) Frequency-tracking responses (b) Corresponding phase-error responses

Fig. 10 Hardware frequency-tracking and phase-error responses



(a) Frequency-tracking responses (b) Corresponding phase-error responses

Fig. 11 Frequency-tracking and phase-error responses to an inductance step in the hardware experiment

To verify the frequency-tracking performance under a load step, the inductance was switched from 149 μH to 144 μH. The experimental results are shown in Fig. 11.

As shown in Fig. 11, the DSOGI-PLL starts at an initial frequency of 20 kHz and gradually decreases the operating frequency according to the fundamental phase error, approaching the resonant frequency corresponding to 149 μH after approximately 40 ms. By contrast, the RLS+DSOGI-PLL directly calculates the feedforward frequency from the identified inductance and rapidly positions the operating frequency near 19.02 kHz, substantially reducing the initial frequency-adjustment time. After the inductance step, the DSOGI-PLL converges toward the new resonant point through phase feedback, whereas the proposed method rapidly adjusts its feedforward frequency to approximately 19.34 kHz using the updated inductance estimate. The frequency-convergence times of the two methods are approximately 9.29 ms and 2.32 ms, respectively. In terms of phase convergence, the proposed method also reduces the convergence time from 18.47 ms for the DSOGI-PLL to 5.60 ms, while reducing the maximum phase error from 3.79° to 1.61°.

To provide a consolidated quantitative comparison, Table 2 summarizes the key parameter-identification and transient frequency-tracking metrics obtained from the simulation and hardware experiments. The identification errors represent the maximum steady-state relative errors under the tested load conditions. For the transient metrics, the arrows indicate the change from the standalone DSOGI-PLL to the proposed RLS+DSOGI-PLL. Because the simulation and hardware experiments employed different load parameters and frequency-error tolerances, the two columns provide complementary validation rather than a direct one-to-one comparison.

Table 2 Quantitative comparison of simulation and hardware results

Metric	Simulation	Hardware
Maximum steady-state resistance identification error	0.045%	1.96%
Maximum steady-state inductance identification error	0.006%	1.14%
Maximum phase error after an inductance step	20.80° → 2.91°	3.79° → 1.61°
Frequency-convergence time after an inductance step	32.98 ms → 2.54 ms	9.29 ms → 2.32 ms

Table 2 shows that the proposed method achieves consistent load-parameter identification in both simulation and hardware experiments. The hardware identification errors are slightly larger than those in simulation, which may be attributable to sampling noise and switching interference, but remain limited to 1.96% for resistance and 1.14% for inductance. For the inductance-step transient, the proposed RLS+DSOGI-PLL reduces the maximum phase error by approximately 86.0% in simulation and 57.5% in hardware. The corresponding frequency-convergence time is reduced by approximately 92.3% and 75.0%, respectively. These results confirm that the proposed feedforward-feedback structure improves frequency repositioning while preserving accurate parameter estimation under practical hardware conditions.

5. Conclusions

This study developed and validated a resonant-frequency tracking method for a phase-shift-modulated series-resonant inverter by combining RLS feedforward estimation with DSOGI-PLL feedback. The RLS algorithm identifies the equivalent resistance and inductance online, and the identified inductance is used to calculate the feedforward resonant frequency. The DSOGI-PLL extracts the fundamental phase of the total RLC voltage and resonant current and provides closed-loop correction for feedforward errors and operating disturbances. The main conclusions are summarized as follows:

(1) The simulation results show that the relative errors of the identified load parameters are below 1%. Under an inductance step change, the proposed method decreases the maximum phase error from 20.80° to 2.91° and reduces the frequency-convergence time from 32.98 ms to 2.54 ms.

(2) In the hardware experiment, the maximum steady-state relative errors were 1.96% for resistance and 1.14% for inductance. After a 60° phase-shift step, the two DSOGI-based methods limited the frequency drift to approximately 93% below that of the Sign-PLL.

(3) When the inductance is switched, the RLS+DSOGI-PLL shortens the frequency-convergence time from 9.29 ms to 2.32 ms and reduces the phase-error peak from 3.79° to 1.61°, while shortening the phase-convergence time from 18.47 ms to 5.60 ms. These results indicate that DSOGI-based fundamental phase detection mitigates locking-point displacement caused by phase-shift changes, whereas RLS feedforward rapidly locates the new resonant frequency after load-parameter changes.

From a practical perspective, keeping the operating frequency close to the updated resonant frequency can limit detuning, reactive current, and circulating energy in the resonant tank. This can help maintain the intended soft-switching margin and reduce the risk of hard-switching-related semiconductor losses. Because efficiency and semiconductor losses were not directly measured in this study, these benefits are presented as expected practical implications rather than quantified experimental results. Future work will focus on further improving the robustness of online parameter identification under measurement noise and load nonlinearities, and on validating the proposed method across a wider range of operating conditions.

Conflicts of Interest

The authors declare no conflict of interest.

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