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A Wide-Band Millimeter-Wave On-Chip Six-Port Reflectometer

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Abstract

Following the previous success of measuring the reflection coefficients of devices under test at 20 GHz, this paper proposes a new six-port reflectometer (SPR) chip that aims to work at 40 GHz. The new SPR is implemented with the 0.13-μm IBM BiCMOS-8HP technology, and the overall chip area is 1.5 mm in width and 1 mm in height. To demonstrate the SPR's excellent performance over a wide band, this study utilizes a programmable tuner to create fifteen different loads for the SPR to measure at 30 GHz, 40 GHz, and 50 GHz, respectively. Among the loads, the programmable tuner serves as an important instrument for producing various sliding terminations, which are essential for calibrating the SPR. Compared with the measurement results of a vector network analyzer, the SPR displays maximum measurement errors of -28.6 dB, -32.4 dB, and -27.7 dB while operating at 30 GHz, 40 GHz, and 50 GHz.

Keywords: Six-port reflectometer, reflection coefficient, millimeter-wave range, vector network analyzer

1. Introduction

The six-port reflectometer (SPR) measurement, which Engen [1] was proposed to measure the scattering parameters and reflection coefficients of devices under test (DUTs). Given its robust performance, the SPR architecture has been continually improved and widely adopted in various applications [2-13], including measurement systems at both the board and chip levels. To highlight the achievements of this study, some comparisons with the latest SPR-related works are briefly provided as follows. Zaichenko [9] proposed the idea of applying the Kalman filter to reduce the signal-processing errors in an SPR. In addition, a field programmable gate array (FPGA) was adopted to substantiate the proposed concept. Staszek [10] proposed an SPR by using nonmatched power detectors. The SPR was implemented on a printed circuit board (PCB) and verified to have a decent performance from 2.2 GHz to 2.6 GHz. Chong [11] proposed a waveguide SPR that works at 2.45 GHz. Barakat [12] proposed a wide-band SPR by using a modified ring power divider and three identical 90-degree hybrid couplers. The SPR was designed on a single-layer PCB and verified to enjoy high performance from 2.6 GHz to 3.8 GHz after calibration.

Regardless of the differences in target operational frequencies and achievable measurement accuracy, all the above works related to SPR were implemented on the board or FPGA level. However, being implemented at higher hierarchies renders the previous works less suitable for the realization of embedded testing aiming to reduce the testing costs of radio frequency (RF) commercial chips. By contrast, Lee [13] proposed a simple on-chip SPR capable of working at 20 GHz. Since the SPR was fabricated as a small chip, embedded testing can be easily realized by placing the SPR near the target DUTs inside a chip. To enable the measurement at an even higher frequency, this research proposes a new SPR chip capable of measuring the reflection coefficients of DUTs in the millimeter-wave range. Specifically, the target center operational frequency of the new SPR is set to be at 40 GHz.

Fig. 1 shows the block diagram of the proposed SPR chip, which is enclosed by the dotted rectangle and consists of six ports, designated from "Port 1" to "Port 6." Among the six ports, "Port 1" and "Port 2" are the primary ports that serve as the

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interfaces to the external world. Specifically, "Port 1" connects the SPR chip to an external signal generator, whereas "Port 2" links the SPR chip to an external DUT whose reflection coefficient is to be measured. As for the remaining ports, "Port 3" to "Port 6," they are inside the SPR chip and responsible for sending RF signals from the SPR core to the four amplitude detectors, "DET3" to "DET6."

The reflection coefficient of the DUT can be measured by using four detectors to sense the power levels of the RF signals at appropriate sites of the SPR core [1]. Specifically, the reflection coefficient can be acquired from the three power ratios, computed by dividing the three power levels measured by three detectors to that measured by the fourth one, which works as the reference. By adopting the power reading from "DET3" in Fig. 1 as the reference, one of the three power rations can be conveniently expressed as

$$|\Gamma - q_4|^2 = K_4(P_4/P_3) \tag{1}$$

where Γ is the reflection coefficient to be measured, q_4 and K_4 are parameters related to the SPR design, and P_4 and P_3 are the incident power levels observed by "DET4" and "DET3."

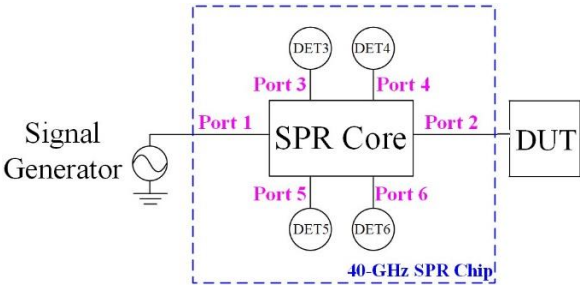

Fig. 1 The block diagram of the proposed SPR chip

Corresponding to the block diagram in Fig. 1, Fig. 2 illustrates the detailed architecture of the proposed SPR chip, which is also inside the dotted rectangle. To emphasize the actual boundary of the SPR, the primary ports, "Port 1" and "Port 2" in Fig. 1, are renamed as the "SPR Port 1" and "SPR Port 2" in Fig. 2. Inside the dotted rectangle, the SPR chip comprises a power divider, a phase shifter, and four amplitude detectors, the DET3, DET4, DET5, and DET6. As can be noted, the "SPR Core" in Fig. 1 is formed by the power divider and phase shifter in Fig. 2. In addition, the exact connections of the four amplitude detectors to the "SPR Core" in Fig. 1 are specifically depicted in Fig. 2. Wiedmann [3] proposed the optimal design requires that the phase shifter create a phase shift of -60 degrees. Additionally, Lee [13] recommended that the impedance looking into each port of the power divider and phase shifter be close to 50 Ω to reduce the effects of mismatch and thus increase the measurement accuracy. Although the new SPR adopts a similar architecture and uses the same fabrication technology as Lee [13], various modifications have been applied to the inner components due to the much higher operational frequency.

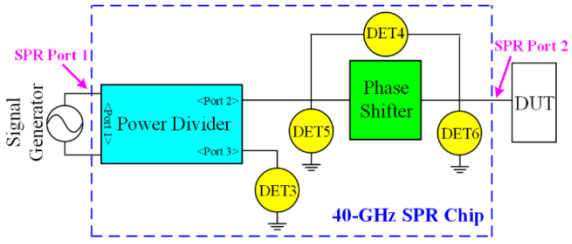

Fig. 2 The architecture of the proposed SPR chip

The SPR proposed by Lee [13] demonstrated high accuracy in measuring the reflection coefficients of various DUTs at 20 GHz. However, the measurement results also revealed a potential weakness of the 20-GHz SPR chip — the excessive signal loss within the SPR. The issue can be visualized in Fig. 17 in Lee's work [13], which shows the magnitude of the S_{21} of the

20-GHz SPR chip. At around 20 GHz, the $|S_{21}|$ is approximately 0.27, lower than the estimation of the original design, 0.5. In addition, it is observable that the $|S_{21}|$ continues to drop as the operational frequency keeps rising. Hence, if the trend of rapid signal decay within the SPR chip is not ameliorated, the SPR may not function normally at 40 GHz because the SPR theorems work on the power levels sensed by the embedded detectors. With such a severe decay, the embedded amplitude detectors may not have sufficient RF signals to detect. Furthermore, the situation is especially stringent for the DET6 since it is the farthest from the signal generator, as revealed in Fig. 2.

To enable the new SPR to work at 40 GHz, the potential problem of excessive signal loss needs to be addressed. This means the components inside the new SPR need to be redesigned. Specifically, this research applies major modifications to the power divider, the phase shifter, and the four embedded amplitude detectors, respectively.

To present the new SPR chip aiming to work at around 40 GHz, the remaining sections are arranged as follows. The major modifications in the new SPR design are presented in Section 2. The experimental results and important discussions are included in Section 3. Finally, the conclusions of this research are presented in Section 4.

2. SPR Design Modifications

To equip the new SPR to operate at the target operational frequency, 40 GHz, some components inside the original SPR of Lee [13] need to be rethought and redesigned. Through careful analysis and trade-offs, this research has decided to make modifications in three main parts — the power diver, the phase shifter, and the amplitude detectors. Each of the three major modifications is detailed as follows.

The first modification is in the power divider. The 20-GHz SPR proposed by Lee [13] adopted a resistive power divider. Such a power divider offers a small layout area at the cost of an extra signal loss of approximately 3 dB around the target operational frequency. As illustrated in Fig. 3, the simulated $|S_{21}|$ and $|S_{31}|$ of the resistive power divider are about -6 dB at around 20 GHz.

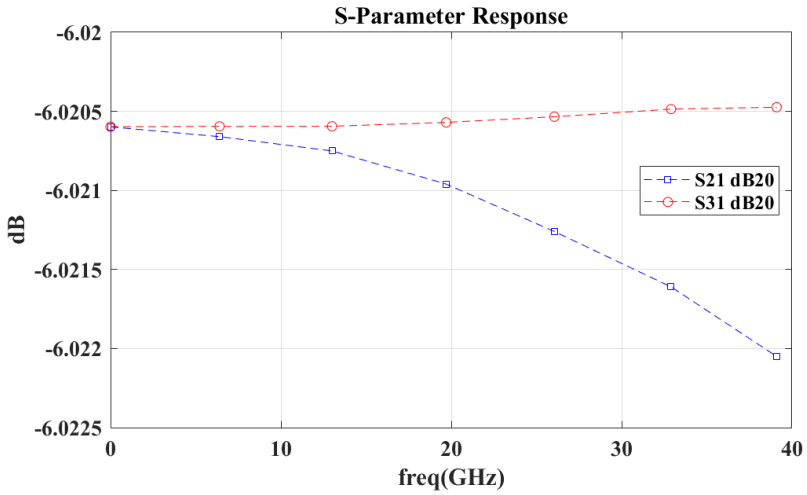

Fig. 3 The simulated $|S_{21}|$ and $|S_{31}|$ of the resistive power divider

Illustrated by Fig. 17 in Lee's work [13], it is known that the real signal attenuation between the SPR Port 1 and SPR Port 2 of the 20-GHz SPR chip was worse than the simulation estimation. In addition, the issue of signal loss can only deteriorate as the operational frequency increases. Hence, if the problem of excessive signal loss in the SPR is not properly addressed, the new SPR may suffer serious imprecision in its measurements when the operational frequency doubles. This is because when the stimulus RF signal is severely attenuated while traveling through the SPR, the signal intensity may become too weak for the detectors to sense. According to the SPR theorems, if any embedded detector fails to measure the power inside an SPR, the SPR will not be able to measure the reflection coefficients.

Given this potential problem, this research attempts to first enhance the RF signal intensity within the new SPR by removing the extra 3 dB loss in the resistive power divider. Using the powerful design tools supported by the IBM BiCMOS-8HP technology, this work adopts a suitable microstrip power divider by considering both performance and layout efficiency. As for the fundamental theorem of a microstrip power divider, readers can consult Xu's work for more information [14]. By replacing the resistive power divider in Fig. 4 by Lee [13] with the adopted one, the signal intensity at the divider's output ports can be theoretically boosted by 3 dB.

Fig. 4 shows the layout of the microstrip power divider, which occupies an area of approximately 400 μm × 460 μm. Fig. 5 shows the simulated $|S_{21}|$ and $|S_{31}|$ of the microstrip power divider, which is approximately -3.6 dB at 40 GHz. This reveals that the microstrip power divider still possesses some internal resistance and thus is not exactly lossless. Compared to the $|S_{21}|$ and $|S_{31}|$ at 20 GHz in Fig. 3, however, those at 40 GHz in Fig. 5 are greatly improved. Hence, at the expense of a larger layout area, the incident power levels observable to the detectors in the SPR are almost doubled by using the microstrip power divider.

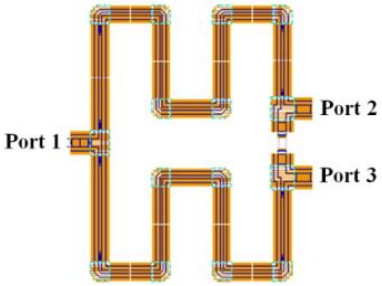

Fig. 4 The layout of the microstrip power divider

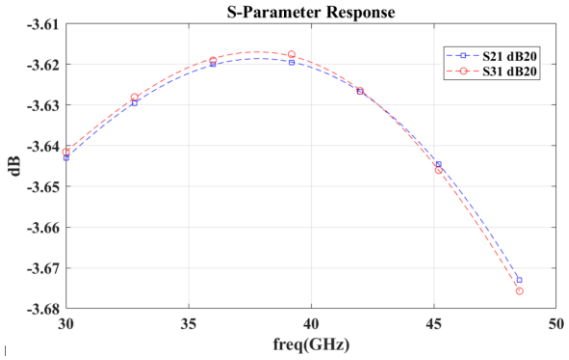

Fig. 5 The simulated $|S_{21}|$ and $|S_{31}|$ of the microstrip power divider

The second modification lies in the phase shifter. The 20-GHz SPR proposed by Lee [13] adopted a lumped phase shifter to cause a phase shift of -60 degrees on the RF signals within the SPR at the operational frequency. To create the same amount of phase shift at 40 GHz, the inductance and capacitance values in Fig. 5 by Lee [13] would become impracticably small to realize. In addition, even if these passive components were fabricated, their diminutive inductance and capacitance values would be very susceptible to the surrounding parasitics. As a result, the overall deviation in inductance and capacitance would then deteriorate the performance of the lumped phase shifter and thus the whole SPR. To avoid these potential problems, this research employs the design tools of the IBM BiCMOS-8HP technology to generate a suitable transmission-line phase shifter by considering both the performance and the required layout area. The adopted transmission-line phase shifter, occupying a rectangular area of approximately 580 μm × 20 μm, is then used to replace the lumped one by Lee [13].

Since the layout area of the lumped phase shifter is about 150 μm × 300 μm, the transmission-line phase shifter enjoys an area reduction of approximately 75%. However, such a nominal reduction may not contribute full advantages in practice. This is because its extreme length, i.e., 580 μm, is unfavorable for placement optimization and likely to cause inevitable area waste as a side effect. The simulated S_{21} of the transmission-line phase shifter is illustrated in Fig. 6. By using the guidelines recommended by Wiedmann [3], the magnitude and phase of the S_{21} are kept close to unity and -60 degrees at around 40 GHz.

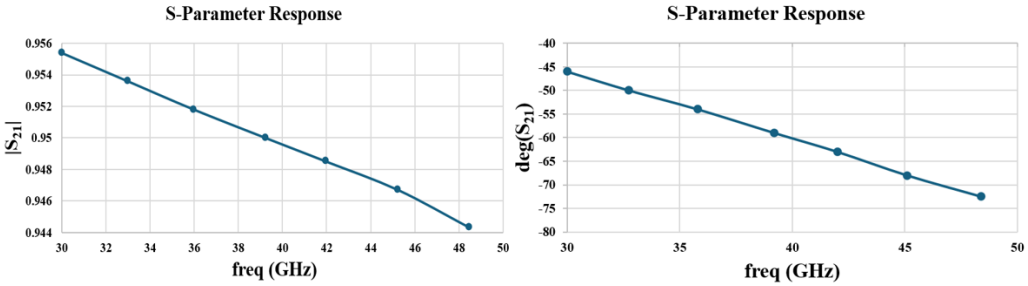

Fig. 6 The simulated S_{21} of the transmission-line phase shifter

The third modification dwells in the amplitude detectors. Fig. 2 in Lee [13] shows a versatile and compact type of amplitude detector with a core of a diode-connected NPN bipolar junction transistor (BJT) embedded in the 20-GHz SPR. In addition, Lee [15] presented that the range of the detector's output DC voltage can be increased by raising the ratio of R_F to R_B. Regarding a given RF signal at the detector's input, a wider range of output is preferable because it means a smaller human error in taking the measurement readings. Hence, this research changes the R_F from 60 kΩ to 120 kΩ while keeping the R_B unchanged, as shown in Fig. 7. With this adjustment, the range of the output DC voltage of the detectors used in the 40-GHz SPR can be approximately doubled.

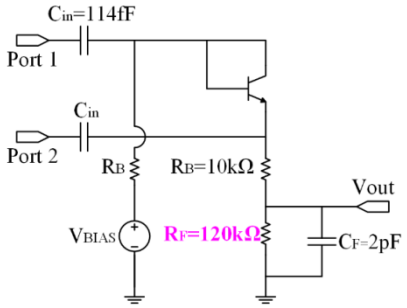

Fig. 7 The schematic and design values of the amplitude detector

3. Experimental Results and Discussion

Corresponding to Fig. 2, Fig. 8 shows the die micrograph of the proposed SPR chip. The SPR circuit is enclosed by the dotted lines, whereas outside the specified area lie the pads and auxiliary test circuitry of other projects. Some of the pads serve as the portals of the SPR, whereas the others are unrelated to the SPR. These unrelated pads work either as dummies that help reinforce the firmness of the chip based on the density rule requirement or as portals for other experimental circuits. It is noteworthy that the area occupied by the SPR is much smaller than the overall chip size, which is 1.5 mm in width and 1 mm in height. This means the SPR will consume much less area when it is used as a means of embedded testing and integrated with target DUTs.

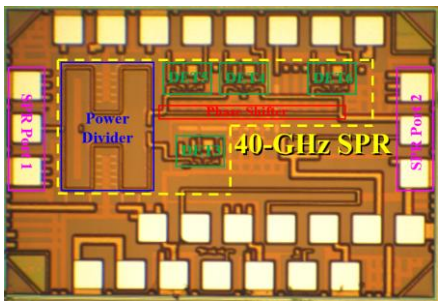

Fig. 8 The die micrograph of the proposed SPR chip

To test the SPR chip, this research adopts the same setup strategy as that illustrated in Fig. 7 by Lee [13]. The SPR chip is fixed on a probe station with at least three arms. Among the three arms, the two opposite ones are used to hold two RF probes, which connect the chip to the external signal generator and programmable tuner. The signal generator functions as the

stimulus by feeding RF sinusoidal signals into the SPR chip. Besides, the programmable tuner serves as the DUTs by creating various loading conditions for the SPR chip to measure. Specifically, this research uses the "Agilent E8257D" as the signal generator and the "Focus Microwaves: Model 67260" as the programmable tuner. As for the third arm of the probe station, it is used to hold a set of DC probes with at least five channels. Among the five channels, one is connected to a power supply to bias the four amplitude detectors, whereas the others are to four voltmeters to read the amplitude detectors' output voltages.

Similar to every SPR, the new SPR chip also needs to be calibrated before it can be used for real measurement. Considering the great measurement results achieved by Lee [13], this research adopts the same calibration procedures, as depicted in Fig. 9 in [13]. In brief, the calibration procedures comprise four main parts—"detector characterization," "initial estimation," "six-port-to-four-port reduction," and "W-to-Γ transformation"—that need to be performed at each measuring frequency. Furthermore, the calibration techniques recommended by Lee [13] are also utilized to enhance measurement accuracy. To prevent redundancy, details of the above calibration procedures and techniques are not particularly emphasized in this paper. Readers are encouraged to consult Lee's work [13] when necessary. To demonstrate the SPR's robust functionalities over a wide band, the proposed SPR chip is also tested at 30 GHz and 50 GHz in addition to the target operational frequency, 40 GHz. The experimental results measured at each operating frequency are detailed as follows.

To start the SPR measurement at 30 GHz, the first step of calibration is to perform the detector characterization. To do so, the programmable tuner is adjusted to generate six loading conditions with reflection coefficients of approximately equal magnitude while having different phases. Loads with such an attribute are often referred to as sliding terminations or sliding loads. For the sake of clarity, the six loading conditions are named from "Load 1" to "Load 6." For each load, the signal generator is set to output a 30-GHz sinusoidal signal with amplitudes sweeping from 0 volts to 1.04 volts with an interval of 80 mV. During the process, the output voltages of each detector are recorded. After all six loads go through the same process, the responses of each detector to different loads and input RF signal amplitudes are available. Fig. 9 summarizes the relationships between the amplitudes of the input RF signals and the detectors' output voltages for the six loads.

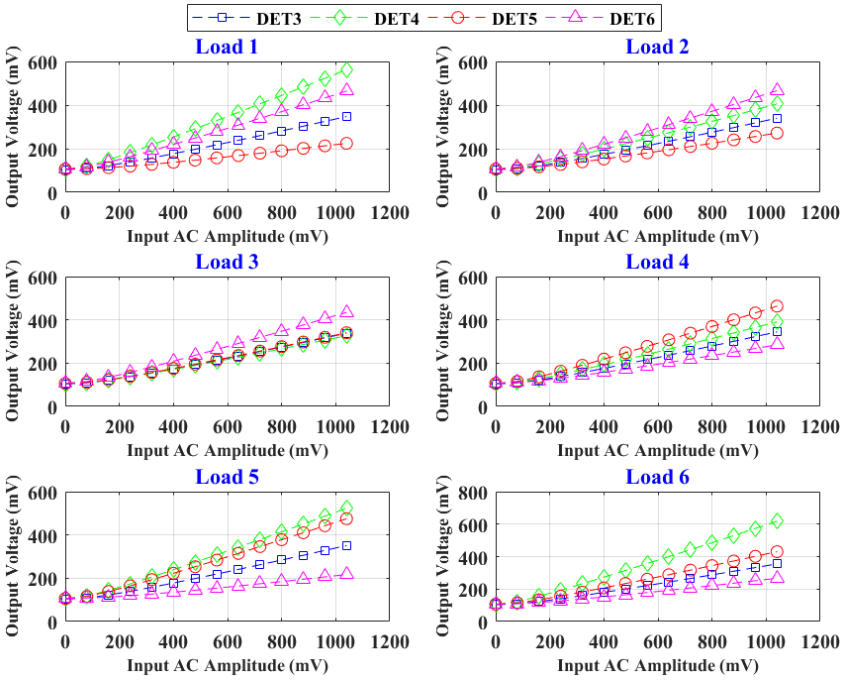

Fig. 9 The detectors' output responses at 30 GHz

By applying the measured voltages in Fig. 9 to the method proposed by Bergeault [16], the detectors can be fully characterized. This means the incident power to a detector's input port(s) can be derived from the detector's output voltage. To reduce possible noise and distortions at extreme input signal amplitudes, the signal generator subsequently fixes the amplitude of its output signal at 640 mV. Concerning the rest of the calibration procedures, this research follows the same

techniques as those presented by Lee [13]. In addition, all six sliding terminations are applied to assist the last step, the "W-to-Γ transformation." To avoid redundancy, this paper omits the executive routines, which can be easily acquired by consulting Lee's work [13]. After the SPR chip is fully calibrated by following the procedures in Fig. 9 of Lee's work [13], it is ready to measure the reflection coefficients of various DUTs.

To enlarge the pool for testing, this research utilizes the programmable tuner to generate nine additional loads, named from "Load 7" to "Load 15." Hence, together with the six sliding terminations, there are a total of fifteen loads used for testing at 30 GHz. The output voltages of each detector concerning "Load 7" to "Load 15" are depicted in Fig. 10. As for the detectors' output voltages corresponding to the six sliding terminations, the values can be acquired by consulting Fig. 9 when the input AC amplitude is 640 mV.

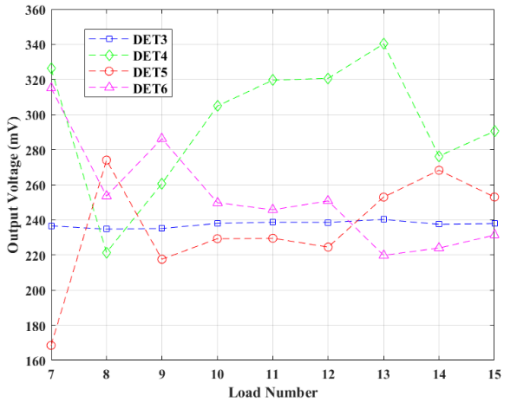

Fig. 10 The amplitude detectors' output voltages at 30 GHz

By applying the measured voltages in Figs. 8 and 9 to the SPR's systemic parameters acquired from the calibration processes, the reflection coefficients measured by the SPR chip can be derived. To know the exact reflection coefficients of the fifteen loads being measured, this research uses a vector network analyzer (VNA), the Agilent E8361A, to measure the output of the programmable tuner. The overall measurement results at 30 GHz are listed in Table 1, where the "Tuner Position" column describes the position commands given to the tuner to create the loads. The "Reflection Coefficient (VNA)" and "Reflection Coefficient (SPR)" columns represent the reflection coefficients measured by the VNA and those by the SPR chip, respectively. Notably, the two columns of data are close to each other, a phenomenon showing the high measurement accuracy of the SPR. Furthermore, the maximum discrepancy in absolute value between the reflection coefficients measured by the VNA and those by the SPR is approximately 0.037, i.e., -28.6 dB, which occurs on the "Load 4."

Table 1 Measurement Results at 30 GHz

Load Number	Tuner Position		Reflection Coefficient (VNA)		Reflection Coefficient (SPR)	
	Pos1	Pos2	Magnitude	Phase (deg)	Magnitude	Phase (deg)
1	1080	2685	0.62931	6.0758	0.64263	8.0136
2	735	2685	0.63186	80.681	0.62571	79.5559
3	585	2685	0.62895	109.73	0.62146	108.2874
4	321	2685	0.59118	157.48	0.60870	160.6068
5	180	2685	0.61578	-168.01	0.60740	-169.5503
6	35	2685	0.61087	-133.15	0.60574	-133.9897
7	900	2685	0.63705	46.747	0.63267	44.5856
8	450	2685	0.60465	132.53	0.58883	134.2334
9	735	2545	0.48859	96.581	0.48520	95.3777
10	586	2124	0.14530	120.99	0.13969	116.7309
11	280	2054	0.06504	148.71	0.05652	141.6378
12	160	1892	0.04761	107.72	0.04691	94.4547
13	198	2388	0.24639	-146.93	0.23791	-146.6249
14	450	2489	0.40343	153.89	0.39131	153.1244
15	463	2373	0.28876	152.02	0.27779	151.014

For better visualization, the measured reflection coefficients in Table 1 are drawn on the Smith chart in Fig. 11. As can be seen, the red stars are in great proximity to the blue circles, a phenomenon reconfirming the great performance of the SPR. It should be explained, however, that the fifteen loads used for testing are created through a trial-and-error mechanism due to the limitation of the programmable tuner. Owing to such limitations, this research found that reflection coefficients in certain regions are difficult to tune. Hence, different from what is normally preferred for demonstration, the reflection coefficients in Fig. 11 are not evenly distributed over the Smith chart.

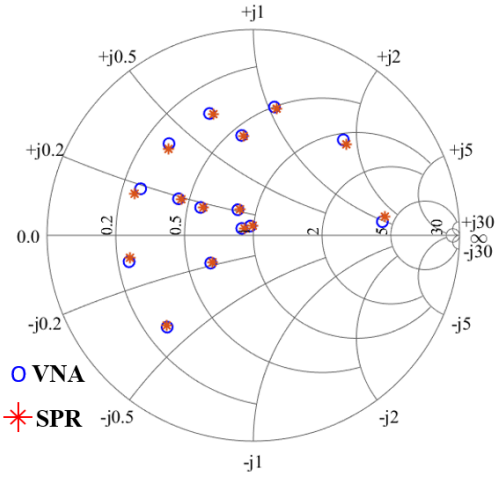

Fig. 11 The reflection coefficients measured at 30 GHz

After the SPR's measurement analysis at 30 GHz is accomplished, the same procedures can be applied to that at 40 GHz and 50 GHz. The repetition of this process ensued hereafter. To test the SPR at 40 GHz, this research uses the programmable tuner to generate fifteen DUTs, named from "Load 1" to "Load 15." To characterize the detectors at 40 GHz, the "Load 1" to "Load 6" are employed. Fig. 12 shows the detectors' output voltages during the detector characterization process.

After the detectors are fully characterized at 40 GHz, this research again fixes the signal generator's output at 640 mV to reduce possible noises and distortions at extreme input signal levels. The rest of the calibration procedures at 40 GHz can be accomplished by utilizing six sliding terminations, the loads numbered 1, 2, 5, 6, 7, and 8. The detectors' output voltages concerning the "Load 7" to "Load 15" are shown in Fig. 13, whereas those corresponding to "Load 1" to "Load 6" can be obtained from Fig. 12.

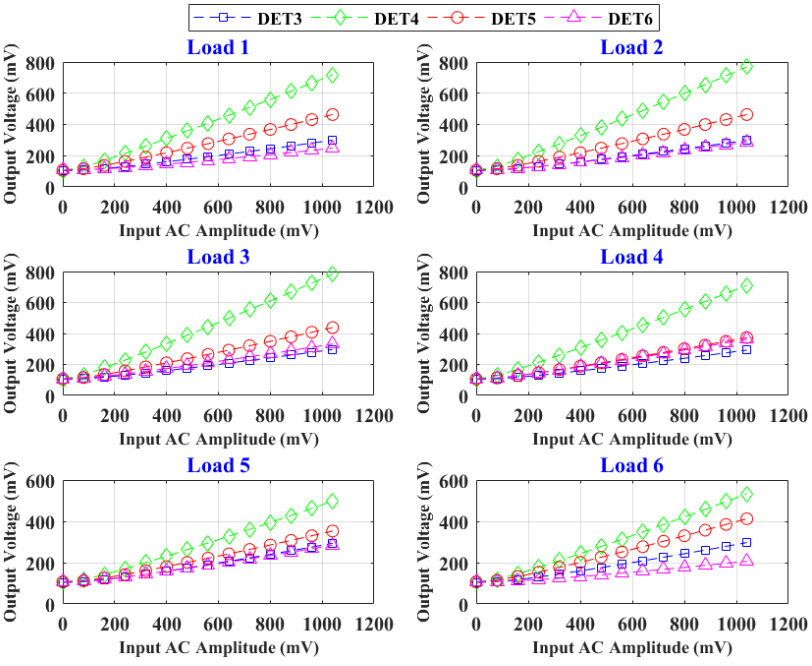

Fig. 12 The detectors' output responses at 40 GHz

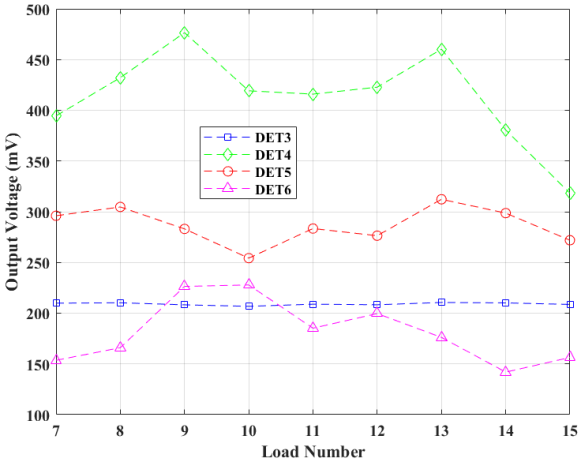

Fig. 13 The amplitude detectors' output voltages at 40 GHz

After all the calibration procedures are performed, the SPR becomes fully calibrated. This means the reflection coefficients measured by the SPR can be derived by applying the detectors' output voltages to the SPR's systemic parameters. The SPR's measurement results at 40 GHz are summarized in Table 2 and graphically depicted in Fig. 14. As can be seen, the SPR chip demonstrates high measurement accuracy. At 40 GHz, the maximum difference in absolute value between the reflection coefficients measured by the VNA and those by the SPR is approximately 0.024, i.e., -32.4 dB, which occurs on the "Load 14."

Table 2 Measurement Results at 40 GHz

Load Number	Tuner Position		Reflection Coefficient (VNA)		Reflection Coefficient (SPR)	
	Pos1	Pos2	Magnitude	Phase (deg)	Magnitude	Phase (deg)
1	1080	2545	0.49024	-82.007	0.49432	-82.6885
2	900	2660	0.50872	-45.745	0.50435	-45.9217
3	735	2680	0.43519	8.2613	0.43123	9.4687
4	585	2680	0.44539	85.209	0.45191	84.4815
5	450	2640	0.50856	153.18	0.50173	153.3233
6	321	2555	0.49102	-163.75	0.49667	-163.4261
7	180	2535	0.51024	-133.47	0.51931	-133.7449
8	35	2535	0.50994	-106.95	0.51670	-108.0575
9	735	2545	0.30154	22.989	0.30214	24.7276
10	585	2545	0.31684	104.64	0.31786	103.8112
11	268	1931	0.17069	-122.5	0.17320	-123.5477
12	650	2208	0.03041	-173.25	0.03158	-173.1591
13	1080	2680	0.59329	-88.694	0.59681	-89.619
14	180	2680	0.61981	-139.66	0.63782	-141.0983
15	321	2680	0.59445	-174.14	0.60136	-172.5347

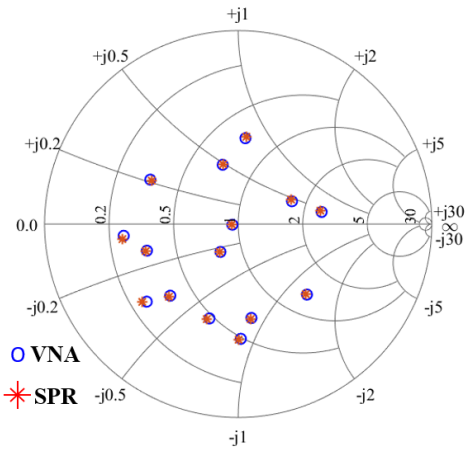

Fig. 14 The reflection coefficients measured at 40 GHz

To test the SPR at 50 GHz, this research uses the programmable tuner to generate fifteen DUTs, named from "Load 1" to "Load 15." To characterize the detectors, the "Load 1" to "Load 6" are first employed. Fig. 15 shows the detectors' output voltages during the characterization process.

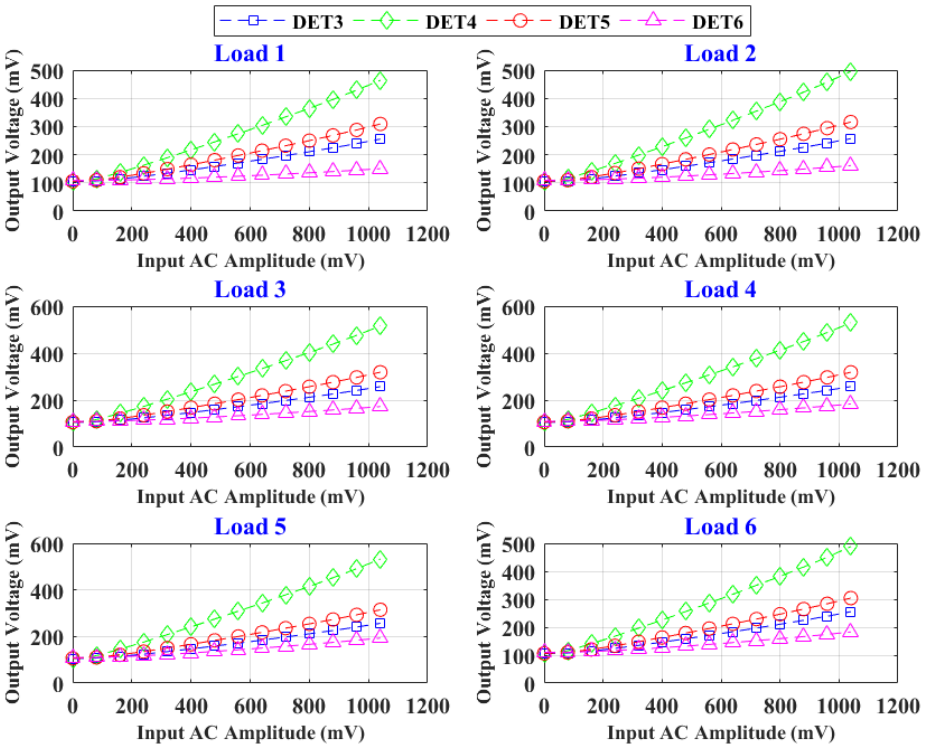

Fig. 15 The detectors' output responses at 50 GHz

After the detectors are characterized at 50 GHz, this research fixes the signal generator's output at 640 mV. As for the rest of the calibration procedures, they are completed by utilizing seven sliding terminations, which are the "Load 1" to "Load 6," and the "Load 8." The detectors' output voltages concerning the "Load 7" to "Load 15" are shown in Fig. 16, whereas those corresponding to "Load 1" to "Load 6" can be obtained from Fig. 15.

After the SPR is fully calibrated at 50 GHz, the reflection coefficients measured by the SPR can be derived by applying the detectors' output voltages to the SPR's systemic parameters. The measurement results at 50 GHz are summarized in Table 3 and graphically illustrated in Fig. 17. Despite slight deterioration, the measurement accuracy of the SPR is still well maintained at 50 GHz. The maximum difference in absolute value between the reflection coefficients measured by the VNA and those by the SPR is approximately 0.041, i.e., -27.7 dB, which occurs on the "Load 10."

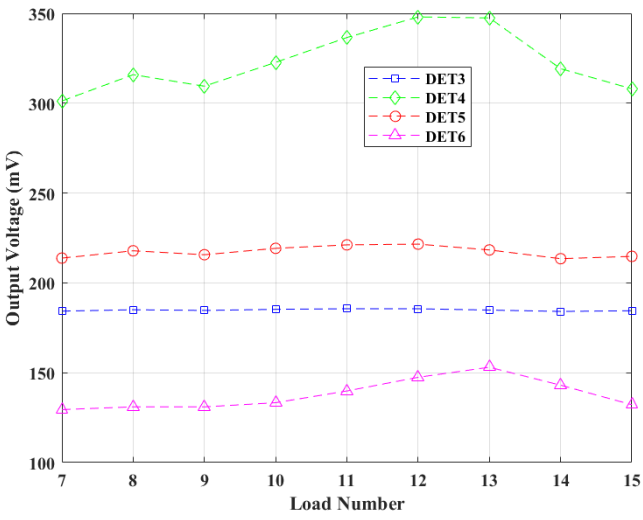

Fig. 16 The amplitude detectors' output voltages at 50 GHz

Table 3 Measurement Results at 50 GHz

Load Number	Tuner Position		Reflection Coefficient (VNA)		Reflection Coefficient (SPR)	
	Pos1	Pos2	Magnitude	Phase (deg)	Magnitude	Phase (deg)
1	1080	2685	0.39518	-104.88	0.40276	-101.0865
2	900	2560	0.40243	-39.485	0.39191	-38.3536
3	735	2480	0.40692	7.7267	0.42849	7.2733
4	585	2490	0.40871	51.732	0.39536	54.5365
5	450	2570	0.40582	102.75	0.41038	101.4599
6	321	2685	0.40378	164.87	0.40322	164.5889
7	180	2685	0.37728	-124.54	0.40346	-128.4482
8	35	2625	0.40817	-65.05	0.40220	-70.4129
9	1080	2545	0.29872	-100.81	0.31286	-107.4347
10	900	2660	0.47132	-40.938	0.45083	-45.3927
11	735	2680	0.55726	4.608	0.52880	3.6457
12	585	2680	0.58003	51.136	0.55183	52.9761
13	450	2640	0.47545	104.64	0.46800	106.264
14	321	2555	0.29876	164.59	0.29572	167.2956
15	180	2535	0.27165	-120.25	0.29973	-124.7056

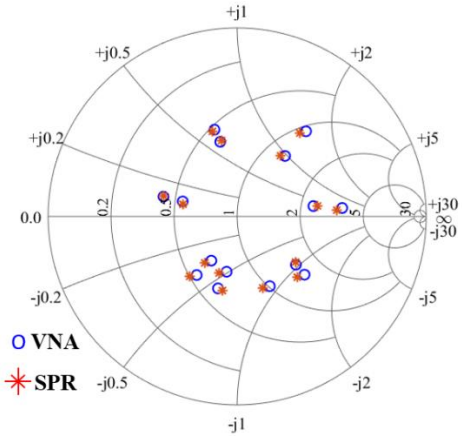

Fig. 17 The reflection coefficients measured at 50 GHz

Based on the measurement results, the SPR chip aiming to work at 40 GHz is confirmed to deliver excellent performance over a wide frequency range. The measurement results at 30 GHz, 40 GHz, and 50 GHz are summarized in Table 4. As can be seen, the maximum measurement error in magnitude is -32.4 dB when the SPR works at the original target frequency, 40 GH. Deviating from 40 GHz, the measurement error begins to worsen in both directions. Specifically, the maximum error reaches -28.6 dB at 30 GHz and -27.7 dB at 50 GHz, causing the bandwidth ratio (f_2/f_1) to be approximately 1.67.

Since most of the recent SPR-related works [9-13] are implemented on the board or FPGA level, comparisons between this research and those works may not provide direct insight. Nevertheless, some key performance indicators are extracted as follows to provide preliminary comparisons. Given that Zaichenko [9] verified the proposed idea through FPGA, the area of chip and board implementation is unavailable. In addition, a concrete report on the measurement error also seems absent. Staszek [10] proposed the board size of the SPR is 106 mm in width and 57 mm in height. The operational band of the SPR ranges from 2.2 GHz to 2.6 GHz, a spectrum causing the bandwidth ratio to be approximately 1.18. Furthermore, the maximum measurement error is 0.0122, which is equivalent to -38.27 dB.

Chong [11] proposed the SPR that works at 2.45 GHz with a three-dimensional size dominated by its rectangular waveguide, which is 109.22mm*54.61mm*300mm. In addition, the maximum error in magnitude was found to be 2.92 dB. Barakat [12] proposed the wide-band SPR that enjoys high performance from 2.6 GHz to 3.8 GHz after calibration, and the spectrum renders the bandwidth ratio approximately 1.46. The size of the fabricated SPR is 11 cm in width and 13.6 cm in

height, whereas the size of the DUT is 4.1 cm in width and 9 cm in height. Since the measurement results are expressed only graphically, the exact numerical error in magnitude is lacking by Barakat [12]. Since the SPR proposed by Lee [13] was measured only at 20 GHz, the bandwidth ratio is unavailable. In addition, the SPR occupies an overall chip area of 1.25 mm in width and 1 mm in height, and the maximum measurement error in magnitude is about -26 dB.

Table 4 Summary of The Measurement Results

Operational Frequency (GHz)	Max$\lvert \Gamma_{SPR} - \Gamma_{VNA} \rvert$	Max$\lvert \Gamma_{SPR} - \Gamma_{VNA} \rvert$ (dB)
30	0.037	-28.6
40	0.024	-32.4
50	0.041	-27.7

By adopting the port definition in Fig. 2, Fig. 18 reveals the $|S_{21}|$ of the SPR chip measured by the VNA. At around 40 GHz, the $|S_{21}|$ is about 0.37, which is much larger than 0.27, the $|S_{21}|$ of the 20-GHz SPR proposed by Lee [13] at approximately 20 GHz. This much improved $|S_{21}|$ also explains the excellent performance of the 40-GHz SPR over a wide band. Despite the greatly enhanced $|S_{21}|$ at 40 GHz, however, 0.37 is still below the original design specification, 0.5. By examining Fig. 18 more closely, it can be noticed that the $|S_{21}|$ is pretty close to 0.5 at around 30 GHz. However, from 30 GHz to 40 GHz, the $|S_{21}|$ starts to decay rapidly, and the rate of decay accelerates from 40 GHz to 50 GHz. Such an accelerating signal decay rate in the SPR as the operational frequency rises poses a potential threat to the accurate measurement of SPR. In addition, the notable signal loss revealed by Fig. 18 also raises a warning to any chip designs aiming to measure the reflection coefficients at higher frequencies.

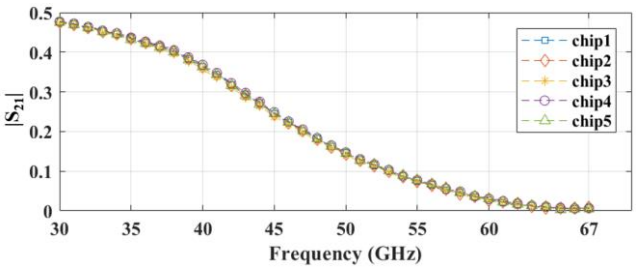

Fig. 18 The measured $|S_{21}|$ of the SPR chip

Nevertheless, the 40-GHz SPR chip succeeds in achieving high measurement accuracy from 30 GHz to 50 GHz despite such a rigorous condition. The success results mainly from three important factors. One is the sound theorems behind the SPR. The second is the reliable semiconductor fabrication technologies nowadays. The third comes from all the modifications aiming to enhance the signal intensity and the system's output observability in the new SPR chip. These modifications, however, come at a price. For instance, the layout area of the microstrip power divider is approximately 92 times the size of the resistive power divider, 40 μm × 50 μm, in Lee's work [13]. In the future, it is predictable that maintaining a sufficient level of signal intensity within the SPR is a key factor and a momentous challenge to accurate measurement at higher frequencies.

4. Conclusions

In this study, an SPR chip that can measure the reflection coefficients of DUTs has been proposed and successfully verified through measurements. As a single chip, the SPR is suitable for placement close to the DUTs of interest—an advantage that enhances measurement accuracy by eliminating irrelevant interface circuitry. The SPR is fabricated in the 0.13-μm IBM BiCMOS-8HP technology with an overall chip area of 1.5 mm in width and 1 mm in height. Notwithstanding the original target operational frequency at 40 GHz, the experimental results confirm that the SPR enjoys excellent measuring accuracy from 30 GHz to 50 GHz. Specifically, the maximum measurement errors in magnitude at 30 GHz, 40 GHz, and 50 GHz are -28.6 dB, -32.4 dB, and -27.7 dB, respectively.

Overall, the proposed SPR possesses decent performance in three aspects—the large bandwidth ratio, the high measurement accuracy, and the small area for chip implementation. Although the measurement accuracy of this research does not surpass all the compared works, the proposed SPR stands out regarding the chip area, which is small and hence extremely favorable for the implementation of embedded testing. Notably, as shown in Fig. 8, the SPR-related circuit occupies less than half the chip size. In the future, the required chip area can be further reduced when the SPR is used as a means of embedded testing, a configuration that requires no pads. In sum, this research realizes the on-chip measurement of reflection coefficients in the millimeter-wave range by using the SPR theorems. To measure the reflection coefficients at even higher frequencies, this research recommends that efforts be spent on reducing the attenuation of the stimulus signals as they travel through the SPR.

Conflicts of Interest

The authors declare no conflict of interest.

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