An Analysis of Managing Sustainable Competitiveness for Semiconductor Manufacturers

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Abstract

Innovative capability is considered inevitable for firms to sustain their competitiveness. In the recent rapidly changing global competition environment, the traditional integrated device manufacturer (IDM) model in semiconductor industry is facing the limitation of sustaining its profitability and competitiveness. IDM's focusing both chip design and manufacturing for various application segments disperse its resources of innovating sustainable competiveness. This study develops an analysis framework with incorporating data envelopment analysis (DEA) approach to measure the efficiency through proper input and output variables setting. This framework aims at providing guidelines for developing firm's business and technology strategies. We conducted a DEA analysis by collecting financial data from twenty-six leading semiconductor manufacturing companies, including twenty IDMs and six foundries. The results reveal that the foundry companies have higher competitive efficiency than those of IDMs. The empirical analysis suggests that adopting the asset-light business model may provide IDMs a better resource allocation and help the increase of relative efficiency scores.

Keywords: Data envelopment analysis, integrated device manufacturer, foundry, efficiency

1. Introduction

The semiconductor industry has grown to be worth more than 300 billion U.S. dollars annually [1]. The industry is driven by continuous strong demand from downstream segments, such as computers, communications equipment, consumer electronics and industrial instruments. As global competition intensifies and commoditization increases, semiconductor companies rightfully conclude that distinctive capabilities by innovating continuously are needed to attain and sustain high performance. Producing the right product in the right quantities at a competitive cost is the keystone of innovation.

The worldwide semiconductor industry is undergoing several forms of business model change. Pure integrated device manufacturer (IDM), asset-light IDM, and pure integrated circuit (IC) design (fabless) are three distinct types of semiconductor business models. The pure IDM model is that a semiconductor company which designs, manufactures, and sells IC products. The asset-light IDM model maintains an internal manufacturing facility and outsources some process development and product manufacturing to silicon contract foundry companies (foundries), which operates a semiconductor fabrication facility (fab) for the purpose of fabricating the designs of other companies. Fabless companies design their own chips but have no production facility so they outsource manufacturing to IDMs or foundries. A symbiotic relationship has been developed between the foundries and the fabless companies as they pushed each other to higher levels of competency [2]. In the past two decades, IDMs' overall share of the semiconductor market dropped sharply from 98% in 1992 to 75% in 2011, while the global fabless companies' share increased 23% from 1992-2011 [3]. The fabless-foundry (de-integration) model has been pretty successful. This de-integration scheme helps both sides on reducing the uncertainties of pricy technology developments. The rapid decline in IDM market shares suggests that the strong competitiveness from fabless companies and foundries makes it hard for IDMs to maintain core competencies in both IC design and IC manufacturing. It is crucial for semiconductor IDMs to understand how the business models and technology innovations they adopted affect their operation performance. The semiconductor industry is an interesting case which now shows rapid but partially disintegrated phenomena in the industry evolution process.

The data envelopment analysis (DEA) introduced by Charnes et al. [4], is a nonparametric, linear programming-based methodology for identifying the relative efficiency of a homogenous set of decision making units (DMUs) in the presence of multiple inputs and outputs. The efficiency score of efficient DMUs is one, while inefficient DMUs score between zero and one [5]. DEA builds an efficient frontier comprising of all the efficient units, thus allowing a comparison of the best performers and providing the firms with guidelines on where and how to improve their capabilities [6].

This study applies DEA to evaluate the performance of 26 leading semiconductor companies which include 20 IDMs and six foundry companies that possess the IC chips manufacturing competency. This analysis identifies the efficient and inefficient semiconductor companies (i.e. the DMUs) by defining the proper output and input factors, and provides business managers a tool for assisting decision making of business model and technology alternatives for their organizations. This paper will detail how managers can use the results to determine areas that need specific attention, and more importantly specifically what those areas need to focus on in order to become as efficient as their peer groups.

The rest of the paper is structured as follows. Section 2 provides the analysis framework for characterizing how a company's performance is affected by business model and

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technology innovations and addressing the DEA model used to measure performance. Section 3 presents the results and discussions. Conclusions are given in the last section.

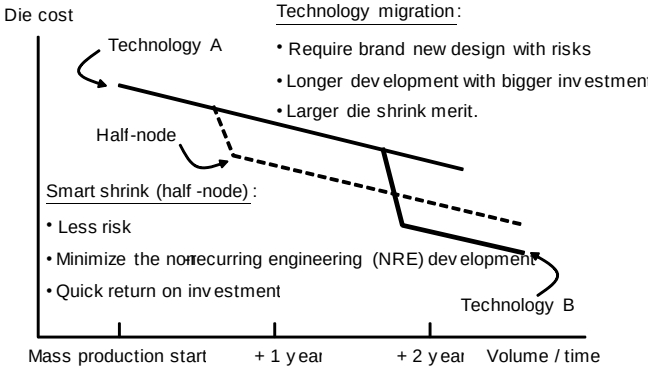

Fig. 1 IC chip's die cost trend for full-node and half-node technologies

2. Research and Theoretical Framework

2.1. Analytical Framework

During the past decade, many IDMs watch closely at unburdening their operations and shift from capital intensive manufacturing to a partial disintegrated asset-light IDM business model. The selection of an appropriate business model needs to be made based on the conditions and constraints specific to the IDMs, such as forceful competition from the rising fabless companies and foundries, escalating R&D costs for developing process technology, and massive investment in manufacturing capacity of state-of-the-art technologies. Further, technology innovation affects semiconductor companies more than other major considerations. For instance, the availability of re-usable intellectual property (IP) blocks affects chip size (i.e. chip cost), the power consumption reduction of power trim technology, the innovative water immersion lithography technique using ultraviolet light at 193 nm wavelength to prolong the equipment life cycle, and the adoption of "half-node" process technology nodes. For example, the process node at 150nm is called a "half-node"—it offers a half step to the next technology node, between 130 and 180 nm. Some foundry customers like to complete their design in one process node and then use a linear, optical shrink to actually fabricate their devices in the half-node. This allows them to take advantage of a unit cost reduction because of a smaller die and also achieve some performance improvement (Fig. 1). Migrating chip design using the smaller shrink factor is less of a challenge, especially if the company plans ahead. Success in implementing such shrinks requires pro-active considerations that allow execution at the half-node with no design rule violations and no yield or reliability issues 2. Business model and technology innovations are continuously being adopted by semiconductor manufacturing companies for sustaining the competitiveness, but it is difficult to do direct evaluation and comparison on the effectiveness and contribution of specific innovations due to the disparate units involved, especially when involving business matters.

This paper develops an analytic framework for semiconductor manufacturers to assist decision making in incorporating business model innovation as an essential part with technology innovation into strategic planning (Fig. 2). Firstly the business and technology strategies of firms could be identified based on the industry features and market trends, e.g. IDM and foundry. Next, firms could further identify the innovations adopted (or to be adopted) corresponding to the selected strategies. Then, the pre-defined relative performance indicators of firms could be evaluated using the DEA technique. Finally, by analyzing the DEA scores and the relationships between performance indicators and the innovations, firms could select salient business strategies for achieving sustainable competitiveness.

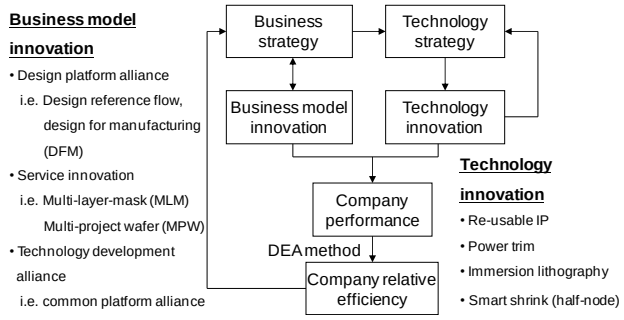

Fig. 2 The analytic framework

2.2. Theoretical Framework

2.2.1 Efficiency Measures by DEA methods

The DEA approach was introduced by Charnes et al. Charnes, Cooper and Rhodes (CCR) model [4] is based on the assumption of constant returns to scale (CRS) when calculating the technical efficiency (TE). Subsequently, Banker et al. [7] proposed the BCC model that assumes variable returns to scale (VRS) and formed a more restricted feasible region than the CCR model. BCC model provides pure technical efficiency (PTE) scores greater than or equal to those obtained assuming CRS. A ratio of TE to PTE provides a measurement of scale efficiency (SE) [8].

Assume that the objective of each DMU is to minimize its inputs, keeping the output level constant in the variable returns to scale (VRS). The pure technical efficiency (PTE) of the target DMU*o* (o=1,…, *n*) can be computed as a solution to the following linear programming problem [9]

$$PTEo = \min \theta_o \quad (1)$$

$$s.t.$$

$$\sum_{j=1}^{n} x_{ij}\lambda_j = \theta_o x_{io}, i = 1,...,m,$$

$$\sum_{j=1}^{n} y_{rj}\lambda_j = y_{ro}, r = 1,...,s,$$

$$\sum_{j=1}^{n} \lambda_j = 1; \lambda_j \geq 0.$$

where n is the number of DMU; m and s are the number of inputs and outputs, respectively. Let x_{ij} and y_{rj} be the amount of the ith input consumed and the amount of the rth output produced by jth DMU, respectively. The PTE of the target DMU*o* is defined as PTE equal to θ_o. By varying the index "o" over all DMUs, we arrive at the PTE in each DMU. If PTE is equal to one, then the DMU*o* is technically efficient. If PTE is smaller than 1, then the DMU*o* is technically inefficient. If $\sum_{j=1}^{n} \lambda_j = 1$ is dropped from Eq. (1), then the technology is said to exhibit constant returns to scale (CRS). The technical efficiency (TE) of the target DMU*o* is defined as TE equal to θ_o under the input-oriented CRS model [4].

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SE equal to unity indicates that this DMU is operating at the most productive scale, in which the TE is equal to the PTE. Otherwise, the DMU could be at decreasing returns to scale if a proportional increase of all input levels produces a less than propositional increase in output levels, and vice versa for increasing return to scales. Refer to reference [11] for more detail about the BCC model.

There is a wealth of literature on both basic and applied research in DEA. It has been widely applied to assess the relative efficiency of organizations, such as the banking industry [10], seaports [11], the high-tech industry [6], and non-profit organizations like a government [12]. It is always a difficult subject for the inefficient DMUs to realize the factors causing the inefficiency, although it is obvious that either reducing inputs or increasing outputs will improve their performances [13]. This study employs the DEA technique to measure technical efficiency (TE), pure technical efficiency (PTE), scale efficiency (SE), and returns of scale (RTS) for each semiconductor company.

Envelope calculations were carried out for each of the two years 2008 and 2009 using the "Learning Version" of DEA-Solver software [14].

2.2.2 Selection of Variables (*Performance Indicators*)

The selection of input and output variables for DEA applications in the semiconductor-related industries can be traced to the literature [6, 15-20]. Chen and Chen [21] noted that the output items should represent the result of the main operations objectives of organizations, and the input items should be the operation factors contributing to the output.

Four input variables are selected for this analysis, which are accessible from public data sources. They are considered the key indicators of managing a firm's competitiveness including both business and technology innovative activities.

- *Total assets* includes total current assets such as inventories and liquid assets of cash, accounts receivable, marketable securities, and total fixed assets such as buildings and structures, machinery and equipment, and investment in securities and common stocks. In general, both IDMs and foundries own high level of total assets because of the nature of semiconductor industry which requires expensive fabrication facilities.
- *Cost of goods sold* (COGS), represents the costs of raw material, labours and related fringe benefits, overhead, depreciation of manufacturing plant and production facilities, rent for land and buildings, and royalties for patent, designs, and other industrial rights. A COG is considered as a tangible value of a company and the difference between the companies' efficiencies.
- *Research and development* (R&D) expenses, represents any expenses associated with the R&D of a company's goods or services. The aim of R&D expenses is immediate invest and to bring the company success in the future. R&D expenses have the characteristic of technology innovation and operation efficiency perspective.
- *Selling, general, and administrative* (SG&A) expenses, includes advertising, sales commissions, distribution-related expenses, sales promotion and other selling expenses, officers' and directors' remuneration and bonuses, payroll, and fringe benefits. The main process perspective is that it helps the company to manage the internal and external part to develop competitive advantages.

The output variable is *net sales*, representing sales revenues of finished goods and merchandise, and operating income from services rendered. Net sales, considered a tangible value of a firm, are the gross increase in owner's equity resulting from business activities. Firms are usually seeking to increase their net sales for economies of scale and cost advantage. Market leaders with a growing market share represent the firms' reputation and clout in the industry

2.3. Sample and Data

We select a sample of 26 leading semiconductor companies (20 IDMs and six foundry companies) with data over the two years 2008 and 2009. The semiconductor market experienced downward cycles in the duration this period. This is an interesting period to study because many semiconductor manufacturers operating in the period had to face industry-wide problems such as enormous R&D expenses for advanced technology development, increase of capital expenditures, new product transitions, design patent protection, unit price erosion, soft demand, production over-capacity, global supply chain problems, and other logistical issues [22]. The list of 26 semiconductor companies contains a broad representation of geographic regions. Each of these companies is treated as a DMU. The memory ICs market had become commoditized due to standardization and excess entry. In addition, Intel Corporation uses in-house manufacturing facilities to fabricate most of the microprocessor chips. Thus, memory companies and Intel haven't been taken into consideration for the sample DMUs. Criteria to select the DMUs are: (1) company's semiconductor sales ranked within top 50 IDM and top 20 foundry market segment in 2009 and (2) individual company's net sales from the semiconductor segment surpassed 50 % of total net sales.

The data of input and output variables are taken from their financial statements which can be accessed through company's investor relations website.

3. Empirical Results and Discussion

3.1. DEA Scores

The results of the DEA pure technical efficiency (PTE), scale efficiency (SE), and the nature of returns to scale (RTS) of each company are shown in Table 1. For the purpose of comparison, sample companies are divided into two main groups, IDM and foundry groups, according to their business models.

Referring to the PTE scores, 26 DMUs could produce the same level of measured output with 7.79-9.67 % less inputs in 2008-2009 on average, holding the current input ratios constant. Approximately 62-65 % of 26 DMUs need to reduce their input if they are to become efficient. The rest of the companies are regarded as efficient. In addition, foundry companies have higher scores on average than IDMs in 2008-2009. The PTE mean scores of IDMs range from 0.8957-0.9110 and foundry firms range from 0.9287-0.9592 in 2008-2009 (Fig. 3). From the "mean" summary of PTE scores, the foundries require 4.08-7.13 % surplus inputs on average in order to achieve the efficient output in 2008-2009 while IDMs requires 8.90-10.43 %, respectively. We consider that IDM model presents relatively insufficient performance because resources are dispersed by taking care of both chip design and manufacturing. In addition, IDMs and foundry companies received higher SE scores than PTE scores in 2008-2009. The result reveals that the overall technical inefficiencies of all the

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IDM and foundry DMUs are caused by inefficient operation rather than the scale inefficiencies. This also suggests that managers should focus firstly on removing the technical inefficiency of a company, and then the company can be subject to improving their scale efficiencies. The dominant effect of scale indicates that most IDMs have been operating at a non-optimal scale of operations.

Table 1 Efficiency scores of the 26 semiconductor companies

DMU	Semiconductor companies	PTE (BCC)		RTS		SE	
		2008	2009	2008	2009	2008	2009
1	Analog Devices, Inc. (U.S.A.)	0.9626	0.9675	CRS	CRS	0.9540	0.8485
2	Advanced Micro Devices, Inc. (U.S.A.)	0.7801	0.8576	CRS	CRS	0.9762	0.9027
3	Atmel Corporation (U.S.A.)	0.9414	0.9459	DRS	CRS	0.9979	0.9991
4	Cypress Semiconductor Corporation (U.S.A.)	0.8702	0.9203	CRS	IRS	0.9467	0.9364
5	Fairchild Semiconductor International, Inc. (U.S.A.)	0.9381	0.9032	DRS	IRS	0.9980	0.9965
6	Freescale Semiconductor, Inc. (U.S.A.)	0.8621	0.8430	IRS	CRS	0.9991	0.9886
7	Infineon Technologies AG (Germany)	0.7595	0.9224	IRS	CRS	0.9992	0.9730
8	Linear Technology Corporation (U.S.A.)	1.0000	1.0000	CRS	CRS	1.0000	1.0000
9	Maxim Integrated Products, Inc. (U.S.A.)	0.9180	0.8934	IRS	IRS	0.9972	0.9993
10	Microchip Technology, Inc. (U.S.A.)	1.0000	0.9638	IRS	IRS	0.9781	0.9689
11	National Semiconductor Corporation (U.S.A.)	0.9740	0.8898	CRS	IRS	0.9953	0.9969
12	NEC Electronics Corporation (Japan)	1.0000	1.0000	DRS	CRS	0.9814	1.0000
13	NXP Semiconductors (Netherlands)	0.6212	0.6557	CRS	CRS	0.9230	0.9925
14	On Semiconductor Corporation (U.S.A.)	0.9392	0.9443	DRS	CRS	0.9974	0.9961
15	Renesas Electronics Corporation (Japan)	0.9373	1.0000	DRS	DRS	0.9062	0.9159
16	ROHM Co., Ltd. (Japan)	0.7150	0.7915	IRS	CRS	0.9986	0.9991
17	Skyworks Solutions, Inc. (U.S.A.)	0.8603	0.8937	IRS	IRS	0.9882	0.9800
18	STMicroelectronics N.V. (Switzerland)	0.8347	0.8285	CRS	CRS	0.9987	0.9893
19	Texas Instruments Incorporated (U.S.A.)	1.0000	1.0000	CRS	CRS	1.0000	1.0000
20	Vishay Intertechnology, Inc. (U.S.A.)	1.0000	1.0000	CRS	CRS	1.0000	1.0000
21	Advanced Semiconductor Manufacturing Co. (China)	1.0000	1.0000	CRS	IRS	1.0000	0.9629
22	China Resources Microelectronics (China)	1.0000	1.0000	CRS	CRS	1.0000	1.0000
23	Taiwan Semiconductor Manufacturing Co. (Taiwan)	1.0000	1.0000	CRS	CRS	1.0000	1.0000
24	United Microelectronics Corporation (Taiwan)	0.8579	1.0000	CRS	DRS	0.9961	0.9966
25	Vanguard International Semiconductor Co. (Taiwan)	1.0000	1.0000	CRS	CRS	1.0000	1.0000
26	TowerJazz Semiconductor (Israel)	0.7145	0.7553	IRS	IRS	0.9500	0.9852
Mean of 20 IDMs (from DMU 1 to DMU 20)		0.8957	0.9110			0.9818	0.9741
Mean of 6 foundry companies (from DMU 21 to DMU 26)		0.9287	0.9592			0.9910	0.9908
Mean of 26 DMUs		0.9033	0.9221			0.9839	0.9780

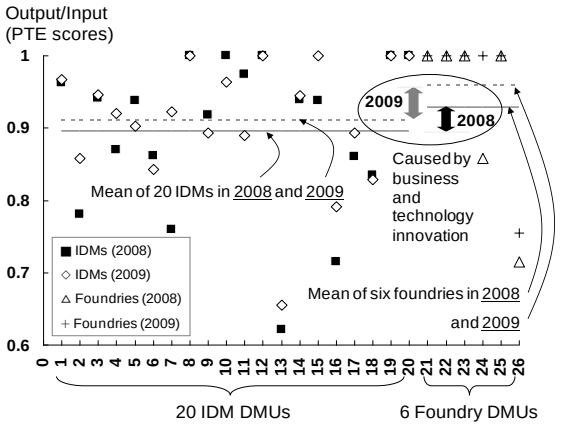

Fig. 3 PTE comparison between selected IDMs and foundry companies

Table 1 reports approximately 75 % of IDM companies and 17-33 % of foundry companies in 2008-2009 (PTE<1) need to reduce their inputs if they are to become efficient. The rest of companies are regarded as efficient (PTE=1). The PTE efficient DMU ratio of all foundry companies increased from 67 % in 2008 to 83 % in 2009. This might be due to the fact that the foundry focuses on IC manufacturing with diversified customer base. It is thus easier for the foundry to be run with a higher efficiency even during downturn. In addition, the gap of mean PTE scores between IDMs and foundries widened in 2009 compared to 2008 (Fig. 3) primarily due to the fierce competition caused by semiconductor downturn from 2008 to 2009. According to the SE scores, three out of 20 IDMs in 2008, four out of 20 IDMs in 2009, four out of six foundries in 2008, and three out of six foundries in 2009 yield scale efficiency. The SE scores of IDMs were worse performer than foundry cluster during 2008-2009. For the lower level scale efficiency (SE) scores of sample DMUs, it could be treated as support for future mergers and acquisitions between firms. To make manufacturing better, faster, and more economical, IDMs could consider unburdening their operations from capital intensive manufacturing to an asset-light IDM business model, if those companies are gradually losing their economies of scale in the semiconductor battleground.

3.2. Returns to Scale

To determine the current operating region for a scale inefficient company, following the result of Zhu and Shen [23], one can easily estimate the returns to scale (RTS) by the TE and PTE scores. If the target company's TE is equal to PTE, then constant return to scale (CRS) prevails; otherwise, the target company indicates decreasing returns to scale (DRS) if a proportional increase of all input levels produces a less than proportional increase in output levels and vice versa for increasing returns to scale (IRS).

Table 1 indicates that 26 DMUs operated with CRS/DRS/IRS mixed patterns. Companies that operated with DRS are too large in scale for their production results. The company scale could be decreased to attempt scale efficiency, if DRS prevail. Companies that operated with IRS are too small in dimension for their production results. Moreover, companies, which have been operating at IRS, could achieve significant cost savings and efficiency gains by increasing its scale of operations. Further mergers and acquisitions among firms to increase the scale of operations could be considered in order to achieve optimal size, significant cost savings, and hence efficiency gains. The results also imply that, in order to reduce the suplus inputs for improving the operational efficiency, the relatively insufficient DMUs with IDM business model could leverage the resources of the efficient DMUs in the foundry companies by adopting the asset-light, or in extremes, the fablessbusiness model.

3.3. DEA Sensitivity Analysis

Table 2 DEA sensitivity analysis results

	20 IDM companies		Six Foundry companies	
	2008	2009	2008	2009
Original TE	0.8801	0.8870	0.9222	0.9506
Inputs excluding total assets				
TE	0.7237	0.7433	0.8901	0.8867
Change %	-18%	-16%	-3%	-7%
Sensitivity Rank	1	1	2	2
Inputs excluding COGS				
TE	0.7590	0.7505	0.9049	0.9325
Change %	-14%	-15%	-2%	-2%
Sensitivity Rank	2	2	4	3
Inputs excluding R&D expenses				
TE	0.8381	0.8433	0.8933	0.9473
Change %	-5%	-5%	-3%	0%
Sensitivity Rank	3	3	3	4
Inputs excluding SG&A expenses				
TE	0.8481	0.8693	0.8260	0.8328
Change %	-4%	-2%	-10%	-12%
Sensitivity Rank	4	4	1	1

In a sensitivity analysis we obtained a different efficient frontier comprising of all the efficient units according to the CCR model under the exclusion of only one of the input variables. The result reflects which key factor influences the DMUs the most. Table 2 reveals that total assets is the significant sensitive indicator for IDM companies from 2008 to 2009, followed by COGS, R&D expenses, and SG&A expenses. Foundry group held SG&A expenses is the

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highest sensitive indicator from 2008-2009, followed by total assets. Foundry companies can get a competitive advantage by skilfully managing the SG&A expenses. Both IDM and foundry groups are capital intensive manufacturers. They fabricate products with a massive depreciation of the equipment. IDM firms can significantly enhance market performance with minimum efforts to leverage foundry's capabilities of R&D and capacity. In today's rapidly evolving world, companies need to constantly adjust their business models to changes in their environment.

4. Conclusions

This research provided an analysis framework of integrating the resource constrains of business model and technology innovations from the firm's financial performances evaluated by DEA model. We properly incorporated four input variables; total asset, COGS, R&D expense, SG&A, and one output; net sales for DEA analysis. We examined the managerial performance efficiency of 26 leading semiconductor companies over the time period of 2008-2009. The results of the DEA analyses show consistency with industry observation. The findings can be briefly summarized as follows.

First, the foundry companies with less resource loss are more efficient on average than IDMs, mainly because foundry companies focus on their core competence in chip manufacturing. Second, the IDM and foundry companies operated with CRS/DRS/IRS mixed patterns. Companies operated at DRS (a proportional increase of all input levels produces a less than proportional increase in output levels) could consider reducing their scale dimension to improve competitive efficiency. IC device manufacturers with prevailing IRS could increase their scale of operation for sustainable competitiveness. Third, foundry group held SG&A expenses are the highest sensitive indicator from 2008-2009, followed by total assets. The IDM group's most significant sensitive indicator is total assets, followed by COGS. The asset-light business model can provide IDMs a better resource allocation and increase relative efficiency scores.

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